JULY 1968

S5400/N7400 SERIES HANDBOOK

S5400J

S5400A

N7400J

N7400A

PRELIMINARY INFORMATION

- Data Sheets
- Logic Diagrams
- Test Circuits

S5400/N7400

SIGNETICS CORPORATION • 811 EAST ARQUES AVENUE, SUNNYVALE, CALIFORNIA 94086 • TEL: (408) 739-7700 • TWX: (910) 399-9220

A SUBSIDIARY OF CORNING GLASS WORKS

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE–AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Supply Voltage V_{CC} (See Note 1) 7V
Input Voltage V_{in} (See Notes 1 and 2) 5.5V
Operating Free-Air Temperature Range S5400 . . . . . −55°C to +125°C
N7400 . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

		MIN.	NOM.	MAX.	UNITS
Supply Voltage, V_{CC} (Note 1)	S54	4.5	5.0	5.5	V
	N74	4.75	5.0	5.25	V
Fan-Out	Gates			10	–
	Buffer			30	

LOGIC DEFINITION

Series 54/74 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0
HIGH VOLTAGE = LOGICAL 1

INPUT–CURRENT REQUIREMENTS

Each input of the multiple-emitter input transistor requires that no more than −1.6mA flow out of the input at a logical 0 voltage level; therefore, one load (N = 1) is −1.6mA maximum. Each input requires current into the input at a logical 1 voltage level. This current is 40μA maximum for each emitter input. Currents into the input terminals are specified as positive values.

FAN-OUT CAPABILITY

Fan-out reflects the ability of an output to sink current from a number of loads (N) at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each standard output is capable of sinking current or supplying current to 10 loads (N = 10). The buffer gate is capable of sinking current or supplying current to 30 loads (N = 30). Load currents (out of the output terminal) are specified as negative values.

ELECTRICAL CHARACTERISTICS

These are guaranteed over the applicable operating free-air temperature range, unless otherwise noted.

UNUSED INPUTS

For optimum switching times, unused gate inputs should be tied in parallel with used inputs or alternatively to a positive voltage source of 2.4V to 5.5V. This eliminates the distributed capacitance associated with the floating input-transistor emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Supply voltage V_{CC}, if regulated to 5.5V maximum, may be used.

If the supply voltage V_{CC} cannot be limited to 5.5V, the following alternatives are recommended¾

a. Connect unused gate inputs to an independent supply voltage source of 2.4V to 5.5V.

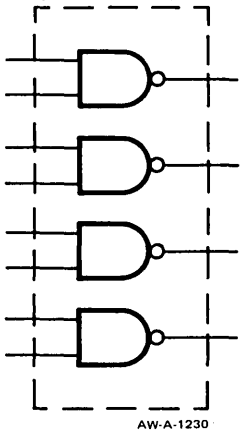
b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded.

In all cases, unused J★ and K★ inputs of the S5470/N7470 must be connected to ground.

Notes:
1. Voltage values are with respect to ground terminals.
2. Input signals must be zero or positive with respect to ground terminal.

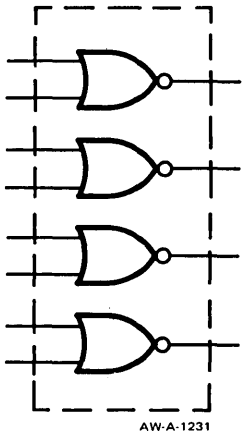
INTEGRATED CIRCUITS

S5400/N7400
S5401/N7401



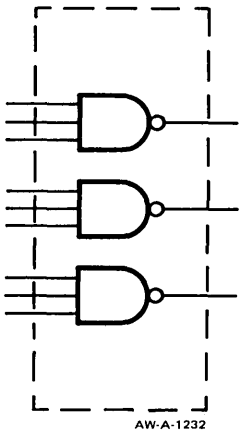
Quadruple 2-Input
Positive NAND Gate

S5402/N7402



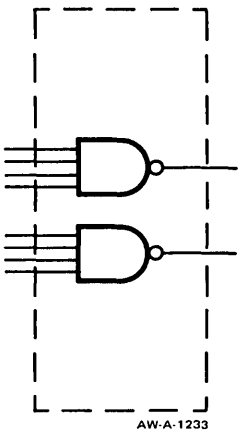
Quadruple 2-Input
Positive NOR Gate

S5410/N7410



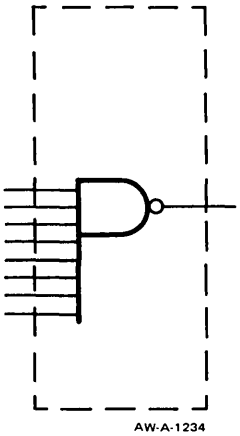
Triple 3-Input
Positive NAND Gate

S5420/N7420



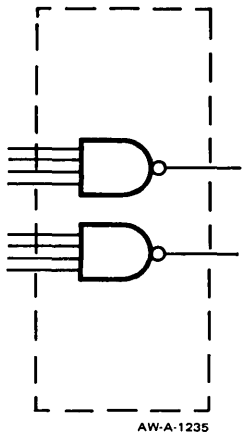
Dual 4-Input
Positive NAND Gate

S5430/N7430



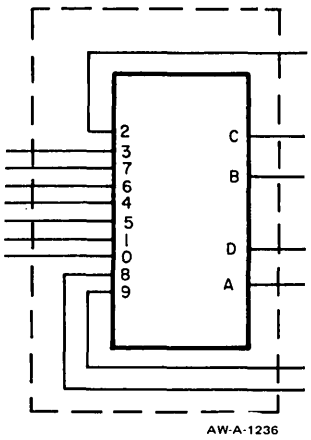
8-Input
Positive NAND Gate

S5440/N7440



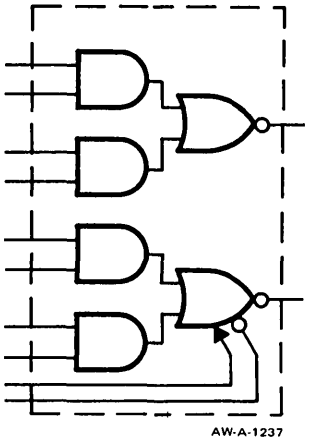
Dual 4-Input
Positive NAND Buffer

S5441/N7441



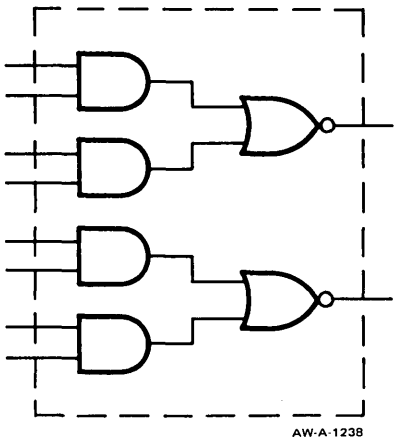
BCD-to-Decimal
Decoder/Driver

S5450/N7450



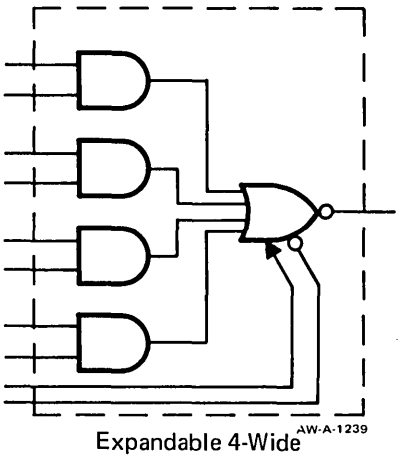
Expandable Dual
2-Wide 2-Input
AND-OR-INVERT Gate

S5451/N7451



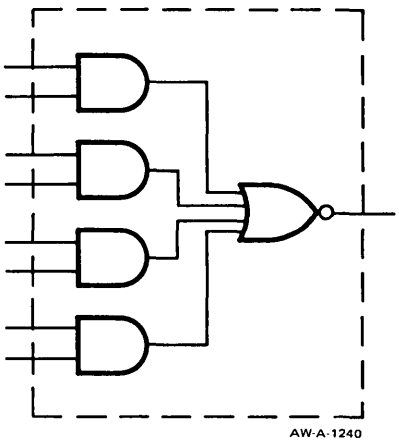
Dual 2-Wide 2-Input
AND-OR-INVERT Gate

S5453/N7453



Expandable 4-Wide
2-Input
AND-OR-INVERT Gate

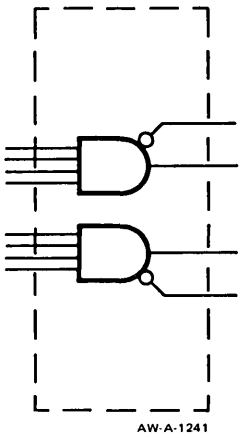
S5454/N7454



4-Wide 2-Input
AND-OR-INVERT Gate

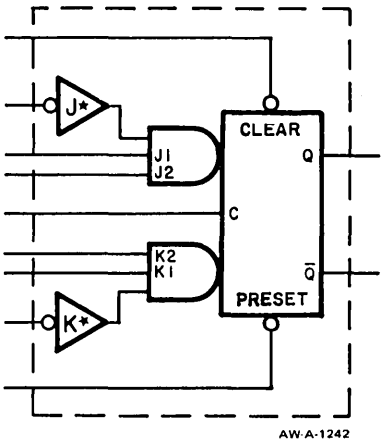
INTEGRATED CIRCUITS

S5460/N7460



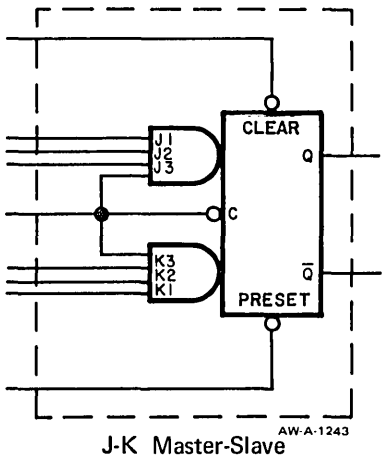
Dual 4-Input Expander

S5470/N7470



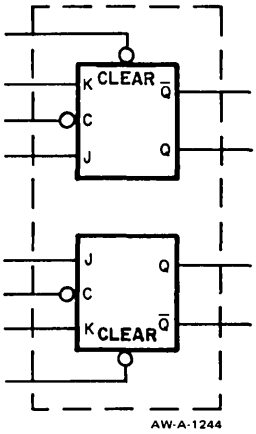
J-K Flip-Flop

S5472/N7472



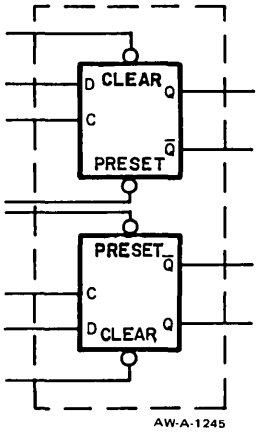
J-K Master-Slave
Flip-Flop

S5473/N7473



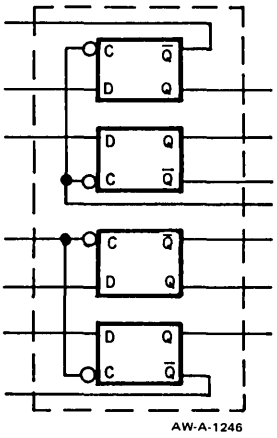
Dual J-K
Master-Slave Flip-Flop

S5474/N7474



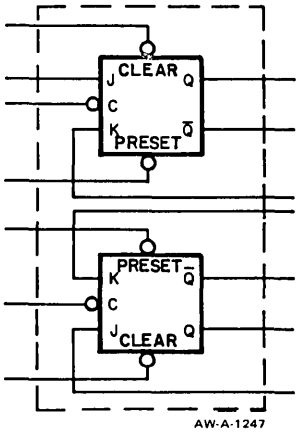
Dual D-Type
Edge-Triggered Flip-Flop

S5475/N7475



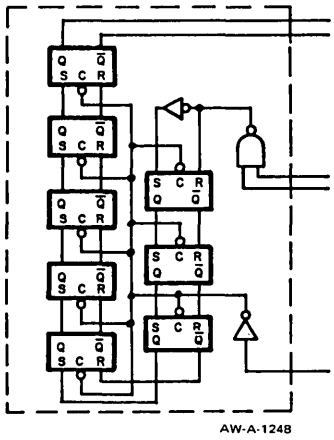
Quadruple Bistable Latch

S5476/N7476



Dual J-K Master-Slave
Flip-Flop with Preset
and Clear

S5491/N7491



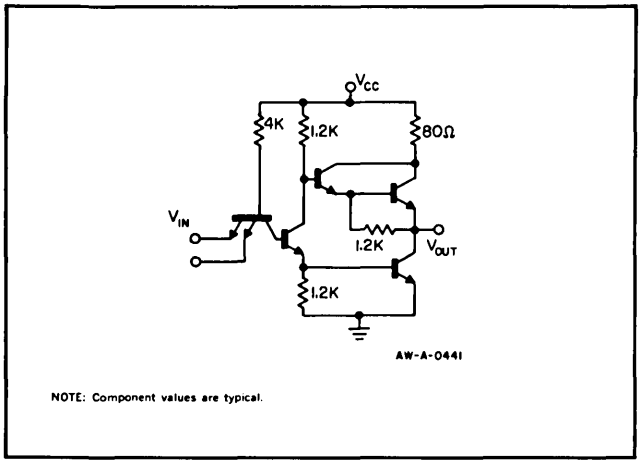
8-Bit Shift Register

NOTE: R=Clear S=Preset

S5400J
N7400J
S5400A
N7400A

QUADRUPLE 2-INPUT POSITIVE NAND GATE

SCHEMATIC (each gate)



NOTE: Component values are typical.

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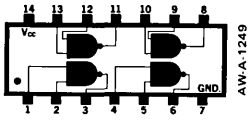

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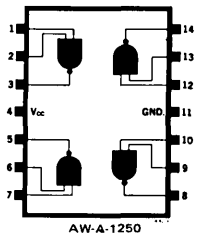


V_{CC} MIN-MAX

ELEMENT	MIN.	NOM.	MAX.	UNIT
S5400A, S5400J	4.5	5	5.5	V
N7400A, N7400J	4.75	5	5.25	V

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS ‡		MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{cc} = Min	$V_{out(0)} \leq 0.4V$	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{cc} = Min	$V_{out(1)} \geq 2.4V$			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{cc} = Min I_{load} = -400 μA	V_{in} = 0.8V	2.4	3.4‡		V
$V_{out(0)}$	Logical 0 output voltage	V_{cc} = Min I_{sink} = 16 mA	V_{in} = 2V		0.18‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{cc} = Max	V_{in} = 0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{cc} = Max	V_{in} = 2.4V			40	μA
I_{os}	Short-circuit output current †	V_{cc} = Max	T_A = 25°C	-18		-75	mA
$I_{cc(0)}$	Logical 0 level supply current (each gate)	V_{cc} = 5V	V_{in} = 5V		4.2‡		mA
$I_{cc(1)}$	Logical 1 level supply current (each gate)	V_{cc} = 5V	V_{in} = 0		1.2‡		mA

† Not more than one output should be shorted at a time.

‡ These typical values are at V_{cc} = 5V, T_A = 25°C.

‡ For conditions shown as MIN or MAX, use value specified in "V_{cc} MIN/MAX" table above.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

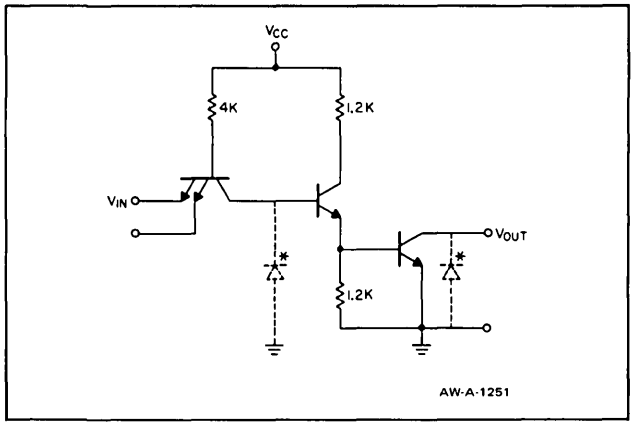
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	1-A	C_1 = 15 pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	1-A	C_1 = 15 pF		8	29	ns

S5401J
N7401J
S5401A
N7401A

QUADRUPLE 2-INPUT POSITIVE NAND GATE

WITH OPEN COLLECTOR OUTPUT

SCHEMATIC (each gate)



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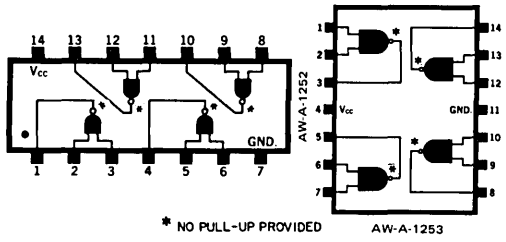


* NO PULL-UP PROVIDED

V_{cc} MIN/MAX

ELEMENT	MIN.	NOM.	MAX.	UNIT
S5401J, S5401A	4.5	5	5.5	V
N7401J, N7401A	4.75	5	5.25	V

DESCRIPTION

This monolithic circuit features the familiar, high-speed, TTL NAND gate with a single-ended, open-collector output transistor. The addition of this gate to the line provides system designers with a TTL circuit for applications where the wired-OR function is necessary or where interfacing with discrete components is required.

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS †	MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on) level at output	V_{cc} = Min. $V_{out(0)} \leqslant 0.4V$ I_{sink} = 16mA	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (Off) level at output	V_{cc} = Min. $V_{out(1)}$ = 5.5V $I_{out(1)}$ = 250 μA			0.8	V
$I_{out(1)}$	Output reverse current	V_{cc} = Min. V_{in} = 0.6V $V_{out(1)}$ = 5.5V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{cc} = Min. V_{in} = 2V I_{sink} = 16mA			0.4	V

† For conditions shown as MIN or MAX, use value specified in "V_{cc} MIN/MAX" table above.

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		TEST CONDITIONS †		MIN.	TYP.	MAX.	UNIT
$I_{in(0)}$	Logical 0 level input current (each input)	V_{cc} = Max.	V_{in} = 0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{cc} = Max.	V_{in} = 2.4V			40	μA
$I_{cc(0)}$	Logical 0 level supply current (each gate)	V_{cc} = 5V	V_{in} = 5V		4.2		mA
$I_{cc(1)}$	Logical 1 level supply current (each gate)	V_{cc} = 5V	V_{in} = 0		1.2		mA

† For conditions shown as MIN or MAX, use value specified in "V_{cc} MIN/MAX" table above.

SWITCHING CHARACTERISTICS, V_{cc} = 5V, T_A = 25°C

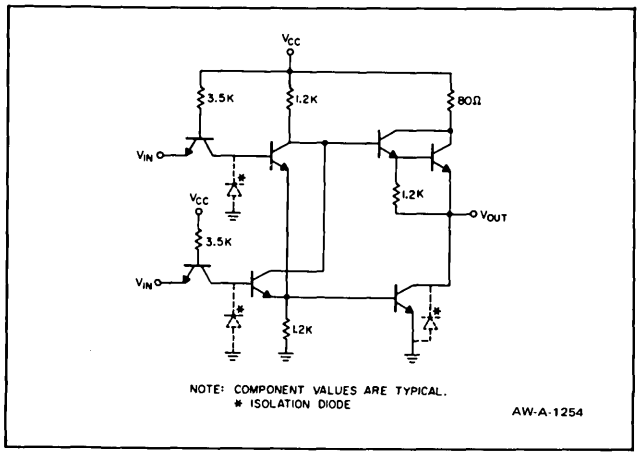
PARAMETER		TEST FIGURE	TEST CONDITIONS ‡	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	1-B	D.C.F.O. = 10			20	ns
t_{pd1}	Propagation delay time to logical 1 level	1-B	D.C.F.O. = 10			45	ns

‡ Load resistor R_L is connected from V_{cc} to the output, and load capacitor C_L is connected from the output to ground.

S5402J
N7402J
S5402A
N7402A

QUADRUPLE 2-INPUT POSITIVE NOR GATE

SCHEMATIC (each gate)



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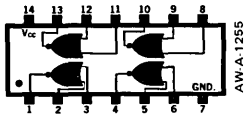

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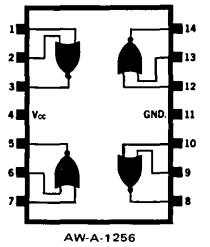


V_{CC} MIN/MAX

ELEMENT	MIN.	NOM.	MAX.	UNIT
S5402J, S5402A	4.5	5	5.5	V
N7402J, N7402A	4.75	5	5.25	V

DESCRIPTION

This monolithic circuit employs standard TTL circuitry, usually implemented to perform NAND logic, to perform a NOR decision. The addition of this gate to the line provides system designers with a TTL circuit for applications where the positive NOR function will reduce the number of logical functions and resultant delay times.

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS†	MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	V_{cc} = Min. $V_{out(0)} \leqslant 0.4V$	2			V
$V_{in(0)}$	Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	V_{cc} = Min. $V_{out(1)} \geqslant 2.4V$			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{cc} = Min. V_{in} = 0.8V I_{load} = −400 μA (See Note 1)	2.4	3.4‡		V
$V_{out(0)}$	Logical 0 output voltage	V_{cc} = Min. V_{in} = 2V I_{sink} = 16 mA (See Note 2)		0.18‡	0.4	V

NOTES: 1. V_{in} is applied to both inputs simultaneously.
2. V_{in} is applied to one input, and the other input is grounded.

† For conditions shown as MIN or MAX, use value specified in "V_{cc} MIN/MAX" table above.

‡ These typical values are at V_{cc} = 5V and T_A = 25°C.

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		TEST CONDITIONS †		MIN.	TYP.	MAX.	UNIT
$I_{in(0)}$	Logical 0 level input current (each input)	V_{cc} = Max.	V_{in} = 0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{cc} = Max.	V_{in} = 2.4V			40	μA
I_{os}	Short-circuit output current ‡	V_{cc} = Max	T_A = 25°C	-20		-75	mA
$I_{cc(0)}$	Logical 0 level supply current (each gate)	V_{cc} = 5V, T_A = 25°C	V_{in} = 5V		4.9		mA
$I_{cc(1)}$	Logical 1 level supply current (each gate)	V_{cc} = 5V, T_A = 25°C	V_{in} = 0		3.5		mA

† For conditions shown as MIN or MAX, use value specified in "V_{cc} MIN/MAX" table above.
‡ Not more than one output should be shorted at a time.

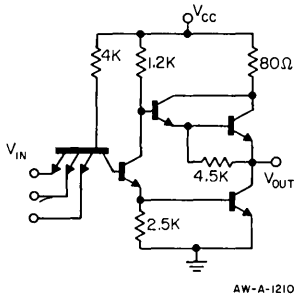
SWITCHING CHARACTERISTICS, V_{cc} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	1-A	C_1 = 15 pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	1-A	C_1 = 15 pF		8	29	ns

S5410J
N7410J
S5410A
N7410A

TRIPLE 3-INPUT POSITIVE NAND GATE

SCHEMATIC (each gate)



NOTE: Component values are typical.

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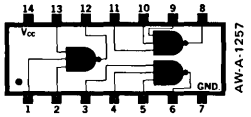

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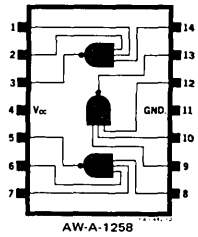


V_{CC} MIN/MAX

ELEMENT	MIN.	NOM.	MAX.	UNIT
S5410A, S5410J	4.5	5	5.5	V
N7410A, N7410J	4.75	5	5.25	V

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS ‡		MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{cc} = Min.	$V_{out(0)} \leqslant 0.4V$	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{cc} = Min.	$V_{out(1)} \geqslant 2.4V$			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{cc} = Min. I_{load} = −400 μA	V_{in} = 0.8V,	2.4	3.4 ‡		V
$V_{out(0)}$	Logical 0 output voltage	V_{cc} = Min. I_{sink} = 16 mA	V_{in} = 2V,		0.18‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{cc} = Max.	V_{in} = 0.4V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{cc} = Max.	V_{in} = 2.4V			40	μA
I_{os}	Short-circuit output current †	V_{cc} = Max.	T_A=25°C	−18		−75	mA
$I_{cc(0)}$	Logical 0 level supply current (each gate)	V_{cc} = 5V,	V_{in} = 5V		4.2‡		mA
$I_{cc(1)}$	Logical 1 level supply current (each gate)	V_{cc} = 5V,	V_{in} = 0		1.2‡		mA

† Not more than one output should be shorted at a time.

‡ These typical values are at V_{cc} = 5V, T_A = 25°C.

‡ For conditions shown as MIN or MAX, use value specified in "V_{cc} MIN/MAX" table above.

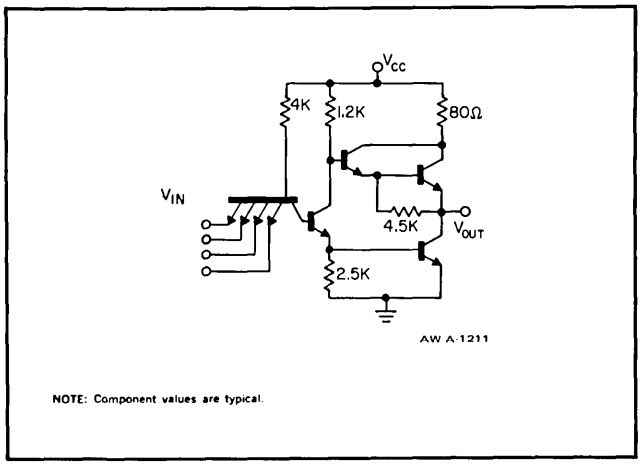
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	1-A	C_1 = 15 pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	1-A	C_1 = 15 pF		8	29	ns

S5420J
N7420J
S5420A
N7420A

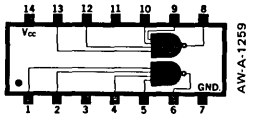
DUAL 4-INPUT POSITIVE NAND GATE

SCHEMATIC (each gate)

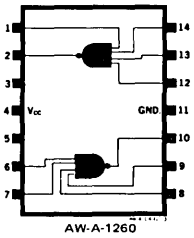


NOTE: Component values are typical.

A PACKAGE



J PACKAGE



V_{CC} MIN/MAX

ELEMENT	MIN.	NOM.	MAX.	UNIT
S5420A, S5420J	4.5	5	5.5	V
N7420A, N7420J	4.75	5	5.25	V

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS ‡	MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{cc} = Min. $V_{out(0)} \leqslant 0.4V$	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{cc} = Min, $V_{out(1)} \geqslant 2.4V$			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{cc} = Min. V_{in} = 0.8V I_{load} = −400 μA	2.4	3.4 ‡		V
$V_{out(0)}$	Logical 0 output voltage	V_{cc} = Min. V_{in} = 2V, I_{sink} = 16 mA		0.18‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{cc} = Max. V_{in} = 0.4V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{cc} = Max. V_{in} = 2.4V			40	μA
I_{os}	Short-circuit output current †	V_{cc} = Max. T_A = 25°C	−18		−75	mA
$I_{cc(0)}$	Logical 0 level supply current (each gate)	V_{cc} = 5V, V_{in} = 5V		4.2‡		mA
$I_{cc(1)}$	Logical 1 level supply current (each gate)	V_{cc} = 5V, V_{in} = 0		1.2‡		mA

† Not more than one output should be shorted at a time.

‡ These typical values are at V_{cc} = 5V, T_A = 25°C, N = 10

‡ For conditions shown as MIN or MAX, use value specified in "V_{cc} MIN/MAX" table above.

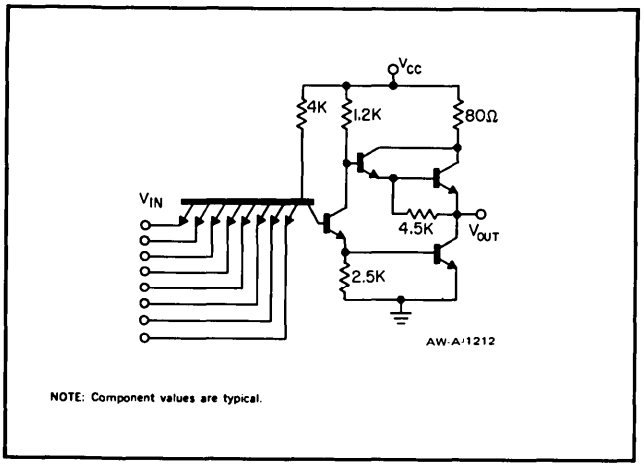
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{pd}0$	Propagation delay time to logical 0 level	1-A	C_1 = 15 pF		8	15	ns
$t_{pd}1$	Propagation delay time to logical 1 level	1-A	C_1 = 15 pF		8	29	ns

S5430J
N7430J
S5430A
N7430A

8-INPUT POSITIVE NAND GATE

SCHEMATIC (each gate)



NOTE: Component values are typical.

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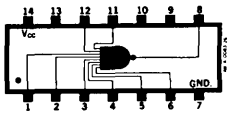
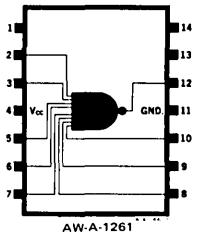


J PACKAGE



V_{CC} MIN/MAX

ELEMENT	MIN.	NOM.	MAX.	UNIT
S5430A, S5430J	4.5	5	5.5	V
N7430A, N7430J	4.75	5	5.25	V

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS ‡		MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{cc} = Min.	$V_{out(0)} \leq 0.4V$	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{cc} = Min.	$V_{out(1)} \geq 2.4V$			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{cc} = Min. $I_{load} = -400\ \mu A$	V_{in} = 0.8V	2.4	3.4‡		V
$V_{out(0)}$	Logical 0 output voltage	V_{cc} = Min. I_{sink} = 16 mA	V_{in} = 2V		0.18‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{cc} = Max.	V_{in} = 0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{cc} = Max.	V_{in} = 2.4V			40	μA
I_{os}	Short-circuit output current	V_{cc} = Max.	T_A = 25°C	-18		-75	mA
$I_{cc(0)}$	Logical 0 level supply current	V_{cc} = 5V	V_{in} = 5V		4.2‡		mA
$I_{cc(1)}$	Logical 1 level supply current	V_{cc} = 5V	V_{in} = 0		1.2‡		mA

‡ These typical values are at V_{cc} = 5V, T_A = 25°C.

‡ For conditions shown as MIN or MAX, use value specified in "V_{cc} MIN/MAX" table above.

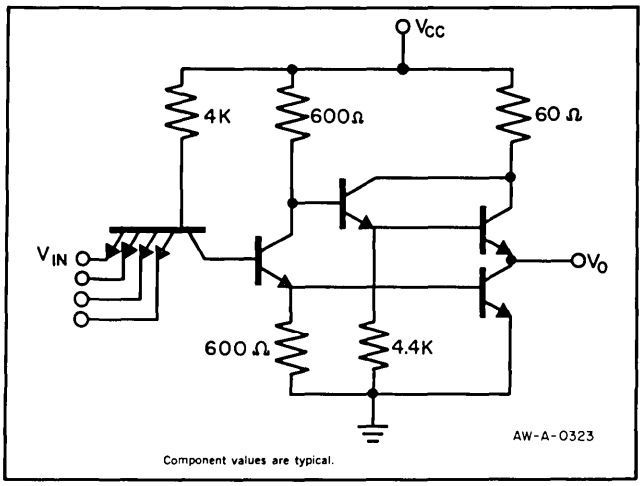
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	1-A	C_1 = 15 pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	1-A	C_1 = 15 pF		8	29	ns

S5440J
N7440J
S5440A
N7440A

DUAL 4-INPUT POSITIVE NAND BUFFER

SCHEMATIC (each gate)



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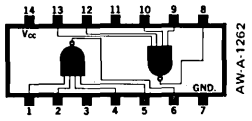

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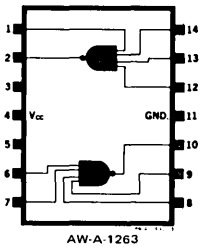


V_{CC} MIN/MAX

ELEMENT	MIN.	NOM.	MAX.	UNIT
S5440J, S5440A	4.5	5	5.5	V
N7440J, N7440A	4.75	5	5.25	V

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS ‡	MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{cc} = Min. $V_{out(0)} \leqslant 0.4V$	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{cc} = Min. $V_{out(1)} \geqslant 2.4V$			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{cc} = Min. V_{in} = 0.8V I_{load} = -1.2 mA	2.4	3.4‡		V
$V_{out(0)}$	Logical 0 output voltage	V_{cc} = Min. V_{in} = 2V I_{sink} = 48 mA		0.32‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{cc} = Max. V_{in} = 0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{cc} = Max. V_{in} = 2.4V			40	μA
I_{os}	Short-circuit output current †	V_{cc} = Max. T_A = 25°C	-18		-85	mA
$I_{cc(0)}$	Logical 0 level supply current (each gate)	V_{cc} = 5V V_{in} = 5V		7.5‡		mA
$I_{cc(1)}$	Logical 1 level supply current (each gate)	V_{cc} = 5V V_{in} = 0		2 ‡		mA

† Not more than one output should be shorted at a time.

‡ These typical values are at V_{cc} = 5V, T_A = 25°C.

‡ For conditions shown as MIN or MAX, use value specified in "V_{cc} MIN/MAX" table above.

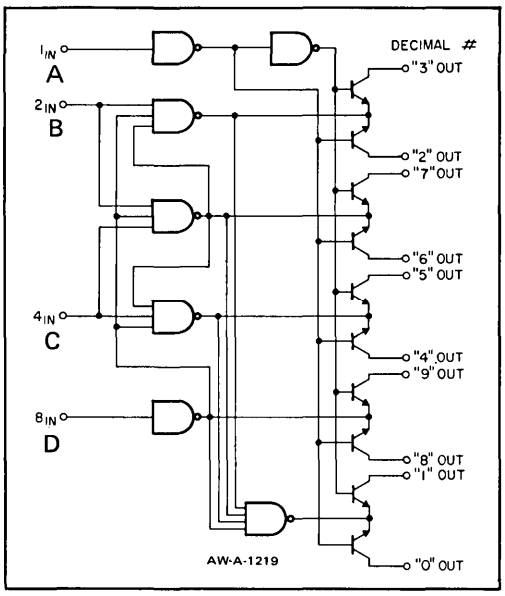
SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 30

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	1-A	C_1 = 15 pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	1-A	C_1 = 15 pF		8	29	ns

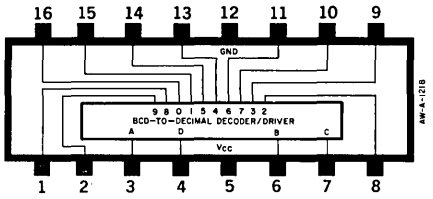
N7441B

BCD-TO-DECIMAL DECODER/DRIVER

LOGIC DIAGRAM



B PACKAGE



V_{CC} MIN/MAX

ELEMENT	MIN.	NOM.	MAX.	UNIT
N7441B	4.75	5	5.25	V

TRUTH TABLE

INPUT				OUTPUT ON ‡
D	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

‡ All other outputs are off.

ELECTRICAL CHARACTERISTICS.

PARAMETER		TEST CONDITIONS †		MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage	V_{cc} = Min.		2			V
$V_{in(0)}$	Logical 0 input voltage	V_{cc} = Min.				0.8	V
V_{on}	On-state output voltage	V_{cc} = Min.	I_{on} = 7mA			2.5	V
I_{off}	Off-state reverse current	V_{cc} = Max.	V_{out} = 55V			200	μA
$I_{in(1)}$	Logical 1 level input current at A or D	V_{cc} = Max.	V_{in} = 2.4V			40	μA
$I_{in(1)}$	Logical 2 level input current at B or C	V_{cc} = Max.	V_{in} = 2.4V			80	μA
$I_{in(0)}$	Logical 0 level input current at A or D	V_{cc} = Max.	V_{in} = 0.4V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at B or C	V_{cc} = Max.	V_{in} = 0.4V			-3.2	mA
I_{cc}	Supply current	V_{cc} = 5V,	T_A = 25°C		15		mA

† For conditions shown as MIN or MAX, use value specified in "V_{cc} MIN/MAX" table above.

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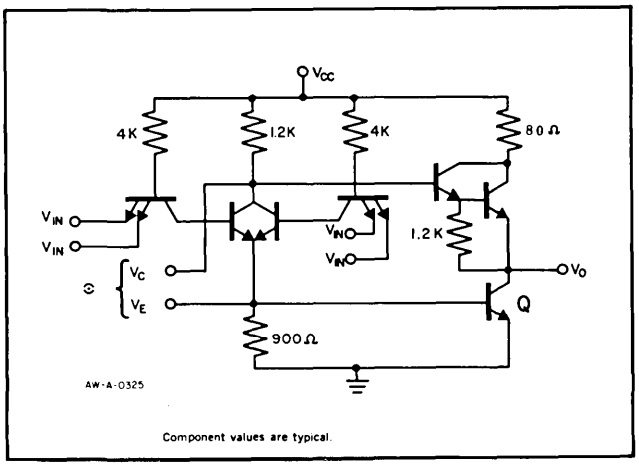
S5450J S5450A N7450J N7450A
S5451J S5451A N7451J N7451A

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

SCHEMATIC (each gate)



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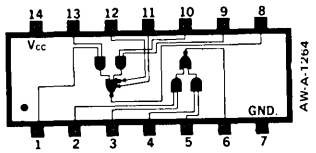
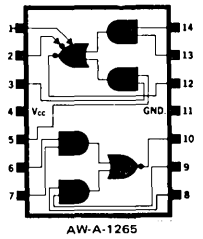


J PACKAGE ◇



◇ Expander nodes not available on S5451/N7451.

V_{CC} MIN/MAX

ELEMENT	MIN.	NOM.	MAX.	UNIT
S5450J, S5450A S5451J, S5451A	4.5	5	5.5	V
N7450J, N7450A N7451J, N7451A	4.75	5	5.25	V

Notes:
1. If expander is not used leave expander pins open.
2. A total of four expander gates may be connected to the S5450/N7450 expander.
3. S5451 pins 1 and 2 open (no expander inputs).
4. N7451 pins 11 and 12 open (no expander inputs).
5. Both S5440/N7450 expander inputs are used simultaneously for expanding with the S5460/N7460.

ELECTRICAL CHARACTERISTICS, Expander Pins Open

PARAMETER		TEST CONDITIONS ‡		MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	V_{cc} = Min.	$V_{out(0)} \leqslant 0.4V$	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	V_{cc} = Min.	$V_{out(1)} \geqslant 2.4V$			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{cc} = Min. I_{load} = −400μA	V_{in} = 0.8V	2.4	3.4‡		V
$V_{out(0)}$	Logical 0 output voltage	V_{cc} = Min. I_{sink} = 16mA	V_{in} = 2V		0.18‡	0.4	V

‡ These typical values are at V_{CC} = 5V, T_A = 25°C.

‡ For conditions shown as MIN or MAX, use value specified in "V_{cc} MIN/MAX" table above.

ELECTRICAL CHARACTERISTICS, Expander Pins Open (Continued)

PARAMETER		TEST CONDITIONS ‡		MIN.	TYP.	MAX.	UNIT
$I_{in(0)}$	Logical 0 level input current (each input)	V_{cc} = Max.	V_{in} = 0.4			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{cc} = Max.	V_{in} = 2.4V			40	μA
I_{OS}	Short-circuit output current †	V_{cc} = Max.	T_A = 25°C	-18		-75	mA
$I_{cc(0)}$	Logical 0 level supply current (each gate)	V_{cc} = 5V	V_{in} = 5V		5.0‡		mA
$I_{cc(1)}$	Logical 1 level supply current (each gate)	V_{cc} = 5V	V_{in} = 0		2.4‡		mA

† Not more than one output should be shorted at a time.
‡ These typical values are at V_{cc} = 5V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use value specified in "V_{cc} MIN/MAX" table above.

SWITCHING CHARACTERISTICS, V_{cc} = 5V, T_A = 25° C, Expander Pins Open, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	1-A	C_1 = 15pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	1-A	C_1 = 15pF		8	29	ns

ELECTRICAL CHARACTERISTICS (S5450/N7450 only) using Expander Inputs.

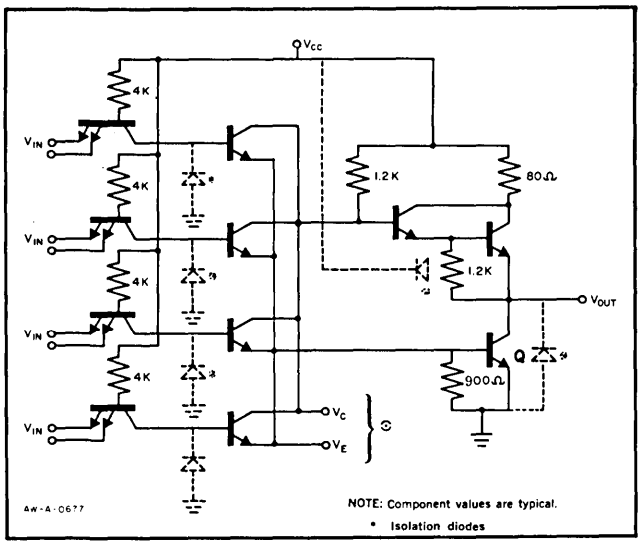
PARAMETER		TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
I_c	Expander current	V_{cc} = Min. I_{sink} = 16mA	V_1 = 0.4V ‡			3.65	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	V_{cc} = Min. I_c = 0.62mA	I_{sink} = 16mA R_1 = 0 ★			1	V
$V_{out(1)}$	Logical 1 output voltage	V_{cc} = Min. I_c = 0.15mA	I_{load} = -400μA I_E = -0.15mA	2.4	3.4‡		V
$V_{out(0)}$	Logical 0 output voltage	V_{cc} = Min. I_c = 0.43mA	I_{sink} = 16mA R_1 = 130Ω ★		0.18‡	0.4	V

‡ These typical values are at V_{cc} = 5V, T_A = 25°C.
‡ $V_1 = V_c - V_E$
★ R_1 is connected between V_c and V_E.

S5453J S5453A N7453J N7453A
S5454J S5454A N7454J N7454A

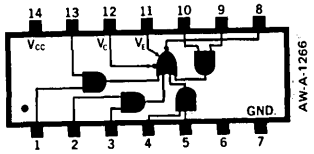
4-WIDE 2-INPUT AND-OR-INVERT GATES

SCHEMATIC (each gate)

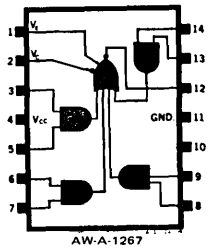


⊜ Expander nodes not available on S5454/N7454

A PACKAGE ⊜



J PACKAGE ⊜



V_{CC} MIN/MAX.

ELEMENT	MIN.	NOM.	MAX.	UNIT
S5453J, S5453A S5454J, S5454A	4.5	5	5.5	V
N7453J, N7453A N7454J, N7454A	4.75	5	5.25	V

Notes:
1. Both S5453/N7453 expander inputs are used simultaneously for expanding with the S5460/N7460.
2. If S5453/N7453 expander is not used, leave expander pins open.
3. A total of four expander gates may be connected to the S5453/N7453 expander inputs.
4. On S5454, pins 1 and 2 are open (no expander inputs).
5. On N7454, pins 11 and 12 are open (no expander inputs).

ELECTRICAL CHARACTERISTICS, Expander Pins are Open.

PARAMETER		TEST CONDITIONS ‡	MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	V_{CC} = Min. $V_{out(0)} \leq 0.4V$	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	V_{CC} = Min. $V_{out(1)} \geq 2.4V$			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = Min. V_{in} = 0.8V I_{load} = −400μA	2.4	3.4‡		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = Min. V_{in} = 2V I_{sink} = 16mA		0.18‡	0.4	V

‡ These typical values are at V_{CC} = 5V, T_A = 25°C.

‡ For conditions shown as MIN or MAX, use value specified in "V_{CC} MIN/MAX" table above.

ELECTRICAL CHARACTERISTICS, Expander Pins are Open (Continued)

PARAMETER		TEST CONDITIONS ‡		MIN.	TYP.	MAX.	UNIT
$I_{in(0)}$	Logical 0 level input current (each input)	V_{cc} = Max.	V_{in} = 0.4			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{cc} = Max.	V_{in} = 2.4V			40	μA
I_{OS}	Short-circuit output current	V_{cc} = Max.	T_A = 25°C	-18		-75	mA
$I_{cc(0)}$	Logical 0 level supply current	V_{cc} = 5V	V_{in} = 5V		5.0‡		mA
$I_{cc(1)}$	Logical 1 level supply current	V_{cc} = 5V	V_{in} = 0		2.4‡		mA

‡ These typical values are at V_{cc} = 5V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use values specified in "V_{cc} MIN-MAX" table above.

ELECTRICAL CHARACTERISTICS (S5453/N7453 only) using Expander Inputs.

PARAMETER		TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
I_c	Expander current	V_{cc} = Min. I_{sink} = 16mA	V_1 = 0.4V ‡			3.65	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	V_{cc} = Min. I_c = 0.62mA	I_{sink} = 16mA R_1 = 0★			1	V
$V_{out(1)}$	Logical 1 output voltage	V_{cc} = Min. I_c = 0.15mA	I_{load} = -400μA I_E = -0.15mA	2.4	3.4‡		V
$V_{out(0)}$	Logical 0 output voltage	V_{cc} = Min. I_c = 0.43mA	I_{sink} = 16mA R_1 = 130Ω★		0.18‡	0.4	V

‡ These typical values are at V_{cc} = 5V, T_A = 25°C
‡ $V_1 = V_c - V_E$
★ R_1 is connected between V_c and V_E

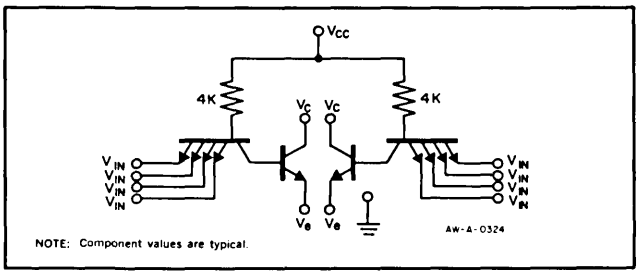
SWITCHING CHARACTERISTICS, V_{cc} = 5V, T_A = 25°C, Expander Pins are Open, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	1-A	C_1 = 15pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	1-A	C_1 = 15pF		8	29	ns

S5460J
N7460J
S5460A
N7460A

DUAL 4-INPUT EXPANDER

SCHEMATIC (each gate)



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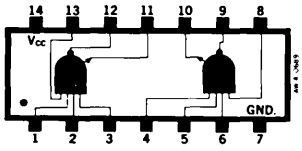
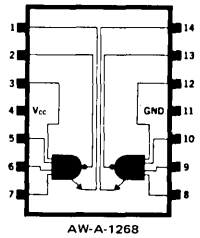


J PACKAGE



V_{cc} MIN/MAX

ELEMENT	MIN.	NOM.	MAX.	UNIT
S5460J, S5460A	4.5	5	5.5	V
N7460J, N7460A	4.75	5	5.25	V

EXPANSION RULES

A PACKAGE:
1. Connect pin 9 or 12 to pin 12 of S5450A/N7450A or S5453A/N7453A.
2. Connect pin 10 or 11 to pin 11 of S5450A/N7450A or S5453A/N7453A.

J PACKAGE:
1. Connect pin 2 or 13 to pin 2 of S5450J/N7450J or S5453J/N7453J.
2. Connect pin 1 or 14 to pin 1 of S5450J/N7450J or S5453J/N7453J.

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS †		MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output on level	V_{cc} = Min. R_1 = 1.1kΩ ‡	V_E = 1V, T_A = 0°C	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output off level current	V_{cc} = Min. R_2 = 1.2kΩ‡	V_1 = 4.5V I_{off} = 0.15 mA			0.8	V
V_{on}	Output voltage on level	V_{cc} = Min. V_E = 1V	V_{in} = 2V R_1 = 1.1kΩ‡			0.4	V
I_{off}	Output off level current	V_{cc} = Min. V_E = 4.5V	V_{in} = 0.8V R_2 = 1.2kΩ‡			270	μA
I_{on}	Output on level current	V_{cc} = Min. V_E = 1V	V_{in} = 2V	-0.43			mA

† For conditions shown as MIN or MAX, use value specified in "V_{cc} MIN/MAX" table above.

‡ R_1 is connected between V_c and V_{cc}.

‡ R_2 is connected between V_E and ground.

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		TEST CONDITIONS †		MIN.	TYP.	MAX.	UNIT
$I_{in(0)}$	Logical 0 level input current (each input)	V_{cc} = Max.	V_{in} = 0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{cc} = Max.	V_{in} = 2.4V			40	μA
$I_{cc(on)}$	On level supply current (each gate)	V_{cc} = 5V V_E = 0.85V	V_{in} = 5V		0.8‡		mA
$I_{cc(off)}$	Off level supply current (each gate)	V_{cc} = 5V V_E = 0.85V	V_{in} = 0		1.2‡		mA

† For conditions shown as MIN or MAX, use value specified in "V_{cc} MIN/MAX" table above.

‡ These typical values are at V_{cc} = 5V, T_A = 25°C

SWITCHING CHARACTERISTICS, V_{cc} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level (through S5450/N7450 or S5453/N7453)	2	C_1 = 15 pF		10	20	ns
t_{pd1}	Propagation delay time to logical 1 level (through S5450/N7450 or S5453/N7453)	2	C_1 = 15 pF		20	34	ns

S5470J
N7470J
S5470A
N7470A

J-K FLIP-FLOP

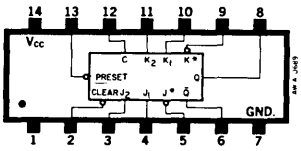
DESCRIPTION

The S5470/N7470 is a monolithic, edge-triggered J-K flip-flop featuring gated inputs, direct clear and preset inputs, and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

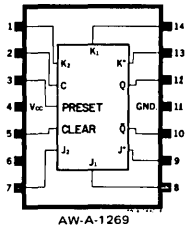
Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse; and after the clock input threshold voltage has been passed, the gated inputs are locked out.

The S5470/N7470 flip-flop is ideally suited for medium- and high-speed applications, and can be used for a significant saving in system power dissipation and package count where input gating is required.

A PACKAGE



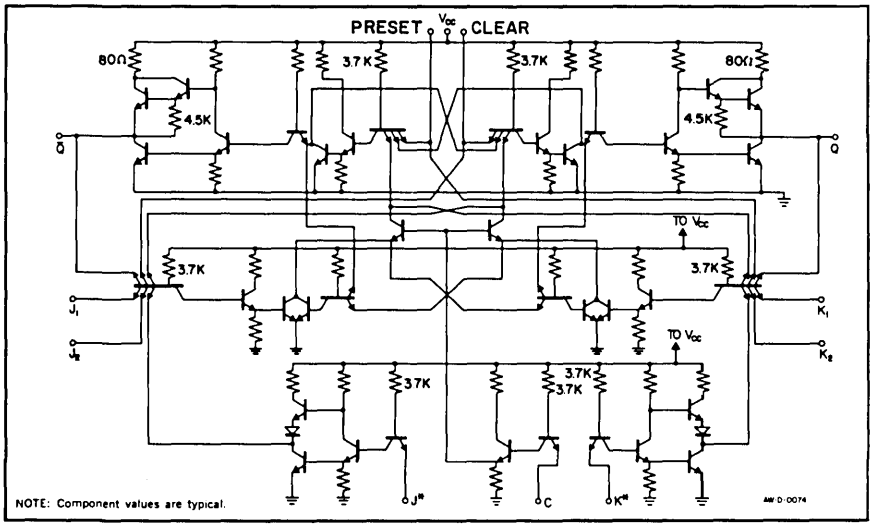
J PACKAGE



POSITIVE LOGIC

Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset or clear function can occur only when clock input is low.

SCHEMATIC



LOGIC

TRUTH TABLE

J_n	K_n	Q_{n+1}	PRESET	CLEAR	Q
0	0	Q_n	0	0	†
1	0	1	1	0	0
0	1	0	0	1	1
1	1	$\overline{Q}_n$	1	1	Q

$J = J_1 J_2 J^\star$ $K = K_1 K_2 K^\star$

n is time prior to clock
n + 1 is time following clock
† Both outputs in 0 state

V_{CC} MIN/MAX.

ELEMENT	MIN.	NOM.	MAX.	UNIT
S5470J, S5470A	4.5	5	5.5	V
N7470J, N7470A	4.75	5	5.25	V

RECOMMENDED OPERATING CONDITIONS

Clock Pulse Transition Time to Logical 1 Level, $t_{1(clock)}$ (See Figure 4). . . . . 5 to 150ns
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 4) . . . . . $\geqslant$ 20ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 3). . . . . $\geqslant$ 25ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 3). . . . . $\geqslant$ 25ns

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS ‡		MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{cc} = Min.		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{cc} = Min.				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{cc} = Min.	I_{load} = −400μA	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	V_{cc} = Min.	I_{sink} = 16mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J*, K1, K2, K*, or clock	V_{cc} = Max.	V_{in} = 0.4V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset or clear	V_{cc} = Max.	V_{in} = 0.4V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J*, K1, K2, K*, or clock	V_{cc} = Max.	V_{in} = 2.4V			40	μA
$I_{in(1)}$	Logical 1 level input current at preset or clear	V_{cc} = Max.	V_{in} = 2.4V			80	μA
I_{os}	Short-circuit output current	V_{cc} = Max.	V_{in} = 0 T_A = 25°C	−18		−75	mA
I_{cc}	Supply current	V_{cc} = 5V	V_{in} = 5V		17‡		mA

‡ These typical values are at V_{cc} = 5V, T_A = 25°C

‡ For conditions shown as MIN or MAX, use values specified in "V_{cc} MIN/MAX" table above.

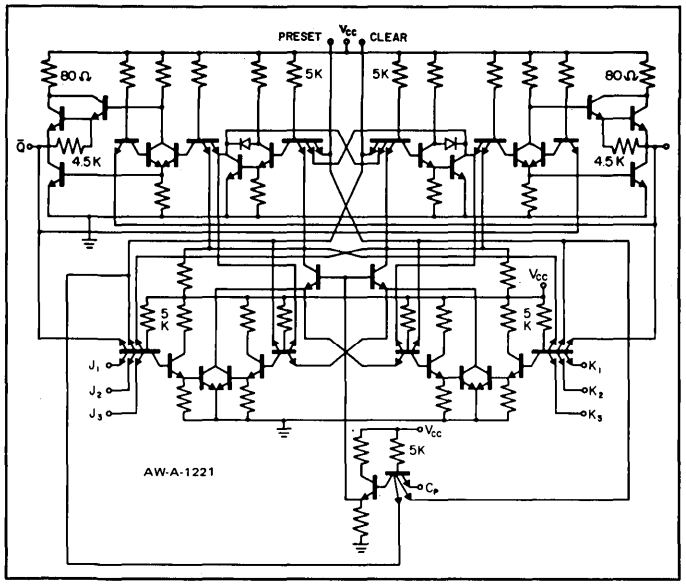
SWITCHING CHARACTERISTICS, V_{cc} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clock}	Maximum clock frequency	4	C_1 = 15pF	15	35		MHz
t_{setup}	Minimum input setup time	4	C_1 = 15pF		10	20	ns
t_{hold}	Minimum input hold time	4	C_1 = 15pF		0	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	3	C_1 = 15pF			50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	3	C_1 = 15pF			50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	4	C_1 = 15pF	10	20	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	4	C_1 = 15pF	10	28	50	ns

S5472J
N7472J
S5472A
N7472A

J-K MASTER-SLAVE FLIP-FLOP

SCHEMATIC



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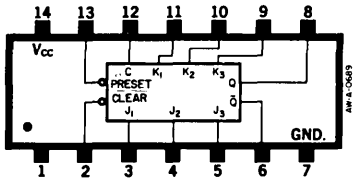

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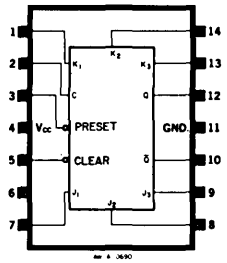


V_{cc} MIN/MAX.

ELEMENT	MIN.	NOM.	MAX.	UNIT
S5472J, S5472A	4.5	5	5.5	V
N7472J, N7472A	4.75	5	5.25	V

LOGIC

TRUTH TABLE

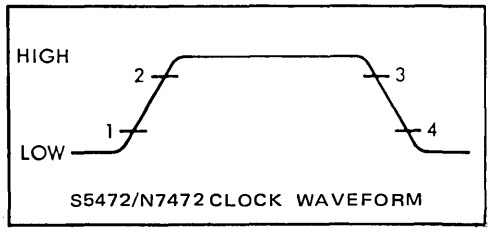
J_n	K_n	Q_{n+1}	PRESET	CLEAR	Q
0	0	Q_n	0	0	†
1	0	1	1	0	0
0	1	0	0	1	1
1	1	$\overline{Q}_n$	1	1	Q

$J = J_1 J_2 J_3$ $\quad K = K_1 K_2 K_3$

n is time prior to clock

n + 1 is time following clock

† Both outputs in 0 state



POSITIVE LOGIC

Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

DESCRIPTION

The S5472/N7472 J-K flip-flop is based on the master-slave principle. This device has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

RECOMMENDED OPERATING CONDITIONS

Width of Clock Pulse, $t_{p(clock)}$ (See Figure 5) . . . . . $\geqslant$ 20ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 6) . . . . . $\geqslant$ 25ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 6) . . . . . $\geqslant$ 25ns
Input Setup Time, t_{setup} (See Figure 5) . . . . . $\geqslant$ Applied Clock Pulse Width
Input Hold Time, t_{hold} . . . . . $\geqslant$ 0

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS ‡		MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{cc} = Min.		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{cc} = Min.				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{cc} = Min.	I_{load} = −400μA	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 out put voltage	V_{cc} = Min	I_{sink} = 16mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, or K3	V_{cc} = Max.	V_{in} = 0.4V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	V_{cc} = Max.	V_{in} = 0.4V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	V_{cc} = Max.	V_{in} = 2.4V			40	μA
$I_{in(1)}$	Logical 1 level input current at preset, clear, or clock	V_{cc} = Max.	V_{in} = 2.4V			80	μA
I_{OS}	Short-circuit output current	V_{cc} = Max.	V_{in} = 0 T_A = 25°C	−18		−75	mA
I_{cc}	Supply current	V_{cc} = 5V	V_{in} = 5V		17‡		mA

‡ These typical values are at Vcc = 5V, T_A = 25°C
‡ For conditions shown as MIN or MAX, use values specified in "V_{cc} MIN/MAX" table above.

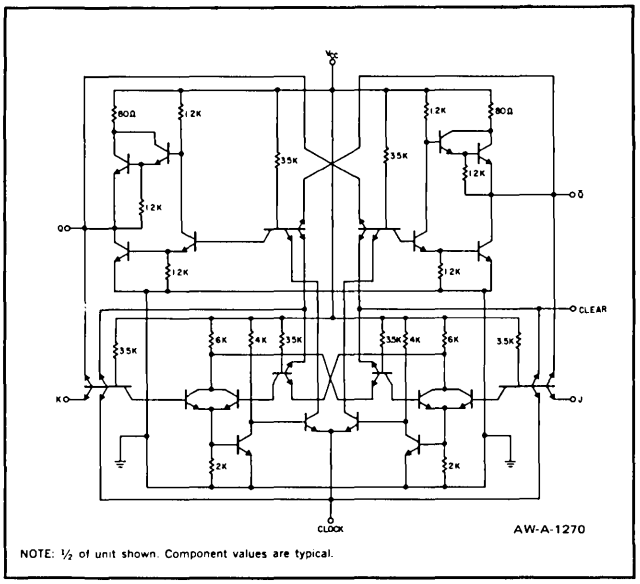
SWITCHING CHARACTERISTICS, V_{cc} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clock}	Maximum clock frequency	5	C_1 = 15pF	10	15		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	6	C_1 = 15pF		26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	6	C_1 = 15pF		34	50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	5	C_1 = 15pF	10	26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	5	C_1 = 15pF	10	34	50	ns

S5473J
N7473J
S5473A
N7473A

DUAL J-K MASTER-SLAVE FLIP-FLOP

SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

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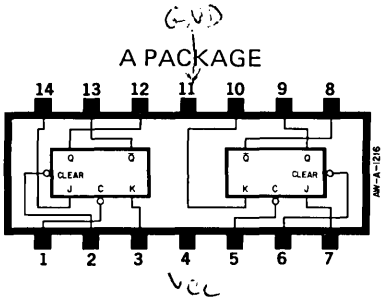

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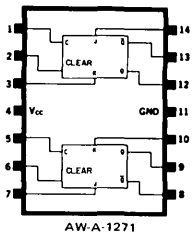


POSITIVE LOGIC

Low input to clear sets Q to logical 0
Clear is independent of clock

LOGIC

TRUTH TABLES

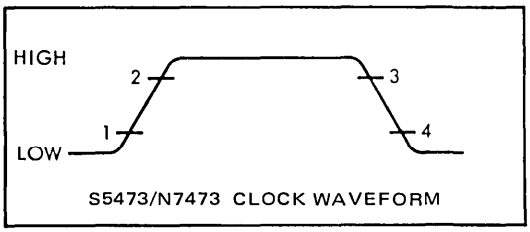
J_n	K_n	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

CLEAR = 0 ⇒ Q = 0

DESCRIPTION

The S5473/N7473 J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.



S5473/N7473 CLOCK WAVEFORM

V_{cc} MIN/MAX.

ELEMENT	MIN.	NOM.	MAX.	UNIT
S5473J, S5473A	4.5	5	5.5	V
N7473J, N7473A	4.75	5	5.25	V

RECOMMENDED OPERATING CONDITIONS

Width of Clock Pulse, $t_{p\,(clock)}$ (See Figure 5) . . . . . ⩾ 20ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 6) . . . . . ⩾ 25ns
Input Setup Time, t_{setup} (See Figure 5) . . . ⩾ Applied Clock Pulse Width
Input Hold Time, t_{hold} . . . . . ⩾ 0

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS ‡		MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{cc} = Min.		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{cc} = Min				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{cc} = Min.	I_{load} = −400μA	2.4	3.4‡		V
$V_{out(0)}$	Logical 0 output voltage	V_{cc} = Min.	I_{sink} = 16mA		0.18‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	V_{cc} = Max.	V_{in} = 0.4V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	V_{cc} = Max.	V_{in} = 0.4V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{cc} = Max.	V_{in} = 2.4V			40	μA
$I_{in(1)}$	Logical 1 level input current at clear or clock	V_{cc} = Max.	V_{in} = 2.4V			80	μA
I_{os}	Short-circuit output current †	V_{cc} = Max.	V_{in} = 0 T_A = 25°C	−18		−75	mA
I_{cc}	Supply current (each flip-flop)	V_{cc} = 5V	V_{in} = 5V		9.5‡		

† Not more than one output should be shorted at a time.
‡ These typical values are at V_{cc} = 5V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use values specified in "V_{cc} MIN/MAX" table above.

SWITCHING CHARACTERISTICS, V_{cc} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clock}	Maximum clock frequency	5	C_1 = 15pF	10	15		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	6	C_1 = 15pF		15	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	6	C_1 = 15pF		25	50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	5	C_1 = 15pF	10	15	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	5	C_1 = 15pF	10	25	50	ns

S5474J
N7474J
S5474A
N7474A

DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

MAY 1968

DESCRIPTION

The S5474/N7474 is a monolithic, dual, D-type, edge-triggered flip-flop featuring direct clear and preset inputs and complementary Q and $\bar{Q}$ outputs. Input information is transferred to the Q output on the positive edge of the clock pulse.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out.

The S5474/N7474 dual flip-flop has the same clocking characteristics as the S5470/N7470 gated (edge-triggered) flip-flop and both are ideally suited for medium- and high-speed applications. The S5474/N7474 can be used at a significant saving in system power dissipation and package count in applications where input gating is not required.

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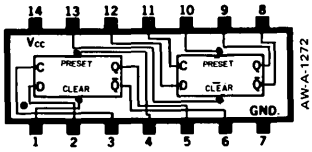
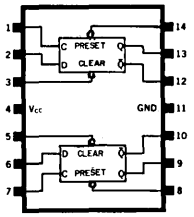


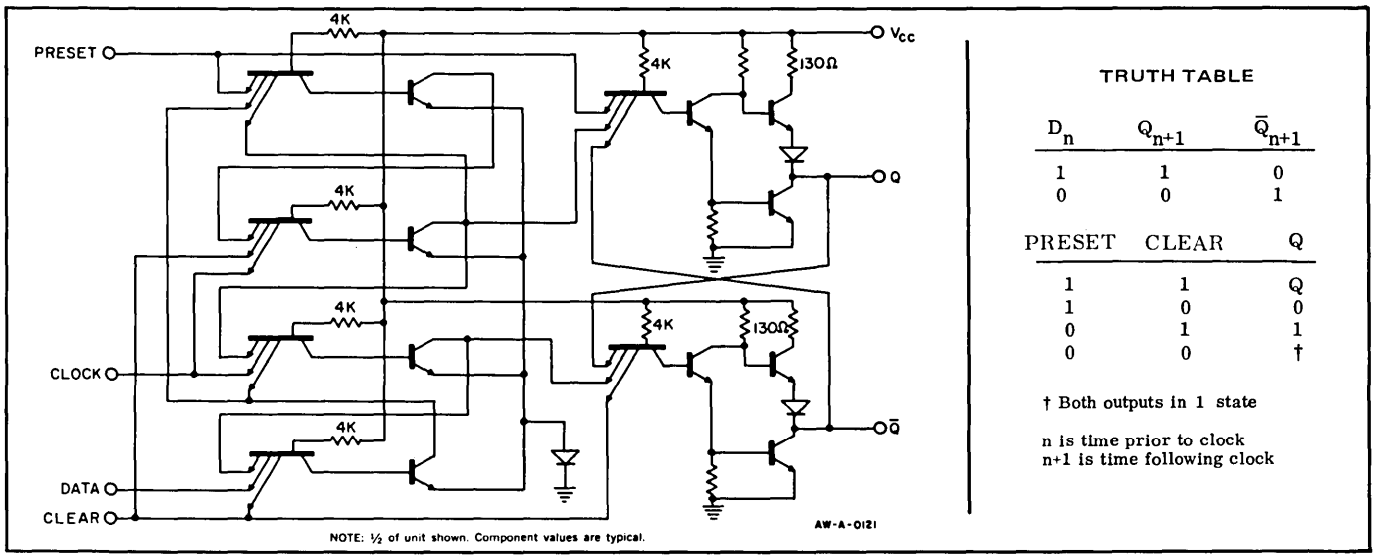
J PACKAGE



POSITIVE LOGIC

Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

TRUTH TABLE

D_n	Q_{n+1}	$\bar{Q}_{n+1}$
1	1	0
0	0	1

PRESET	CLEAR	Q
1	1	Q
1	0	0
0	1	1
0	0	†

† Both outputs in 1 state

n is time prior to clock
n+1 is time following clock

RECOMMENDED OPERATING CONDITIONS

Width of Clock Pulse, $t_{p\,(clock)}$ (See Figure 7) . . . ⩾ 30ns
Width of Preset Pulse, $t_{p\,(preset)}$ (See Figure 4) . . ⩾ 30ns
Width of Clear Pulse, $t_{p\,(clear)}$ (See Figure 4) . . . ⩾ 30ns

V_{CC} MIN/MAX.

ELEMENT	MIN.	NOM.	MAX.	UNIT
S5474J, S5474A	4.5	5	5.5	V
N7474J, N7474A	4.75	5	5.25	V

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS ‡		MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{cc} = Min.		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{cc} = Min.				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{cc} = Min.	I_{load} = −400μA	2.4	3.4‡		V
$V_{out(0)}$	Logical 0 output voltage	V_{cc} = Min.	I_{sink} = 16mA		0.18‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at preset or D	V_{cc} = Max.	V_{in} = 0.4V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	V_{cc} = Max.	V_{in} = 0.4V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at D	V_{cc} = Max.	V_{in} = 4.5V			40	μA
$I_{in(1)}$	Logical 1 level input current at preset or clock	V_{cc} = Max.	V_{in} = 2.4V			80	μA
$I_{in(1)}$	Logical 1 level input current at clear	V_{cc} = Max.	V_{in} = 2.4V			120	μA
I_{os}	Short-circuit output current †	V_{cc} = Max.	V_{in} = 0 T_A = 25°C	−18		−75	mA
I_{cc}	Supply current (each flip-flop)	V_{cc} = 5V	V_{in} = 5V		14‡		mA

† Not more than one output should be shorted at a time.
‡ These typical values are at V_{cc} = 5V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use values specified in "V_{cc} MIN/MAX" table above.

SWITCHING CHARACTERISTICS, V_{cc} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clock}	Maximum clock frequency	7	C_1 = 15pF	15	25		MHz
t_{setup}	Minimum input setup time	7	C_1 = 15pF		15	20	ns
t_{hold}	Minimum input hold time	7	C_1 = 15pF		2	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	4	C_1 = 15pF			25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	4	C_1 = 15pF			40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	7	C_1 = 15pF	10	20	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	7	C_1 = 15pF	10	28	50	ns

S5475B
N7475B

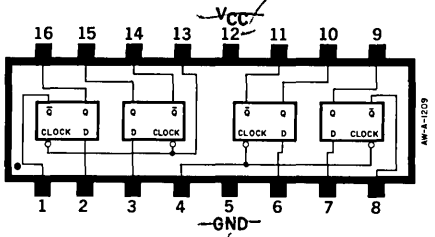
QUADRUPLE BISTABLE LATCH

DESCRIPTION

The S5474B/N7475B is a monolithic, quadruple, bistable latch with complementary Q and $\overline{Q}$ outputs. Information Present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

This latch is ideally suited for use as temporary storage for binary information between processing units and input/ output or indicator units.

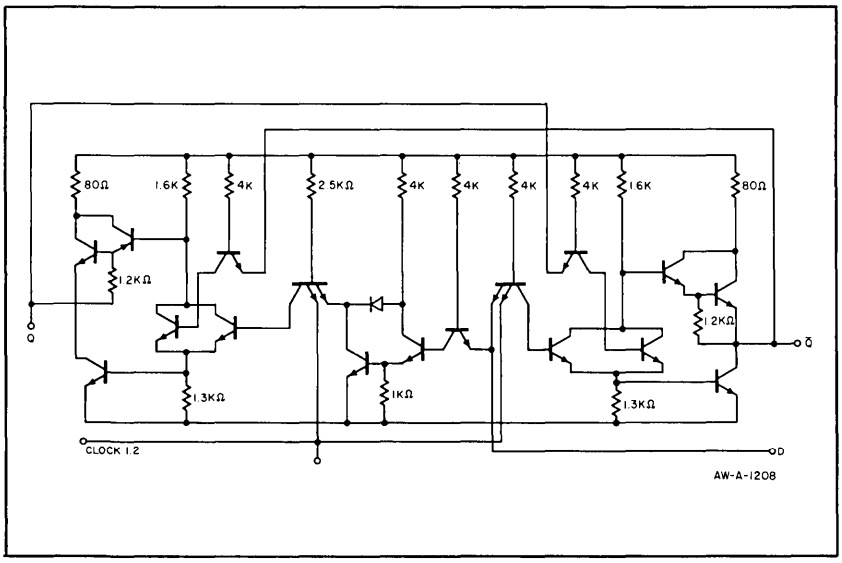
B PACKAGE



V_{CC} MIN/MAX.

ELEMENT	MIN.	NOM.	MAX.	UNIT
S5475B	4.5	5	5.5	V
N7475B	4.75	5	5.25	V

SCHEMATIC (EACH LATCH)



LOGIC

TRUTH TABLE (Each Latch)		
t_n	t_{n+1}	
D	Q	$\overline{Q}$
1	1	0
0	0	1

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS ‡	MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal	V_{CC} = Min.	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal	V_{CC} = Min.			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = Min. I_{load} = −400μA	2.4			V

ELECTRICAL CHARACTERISTICS (Continued)

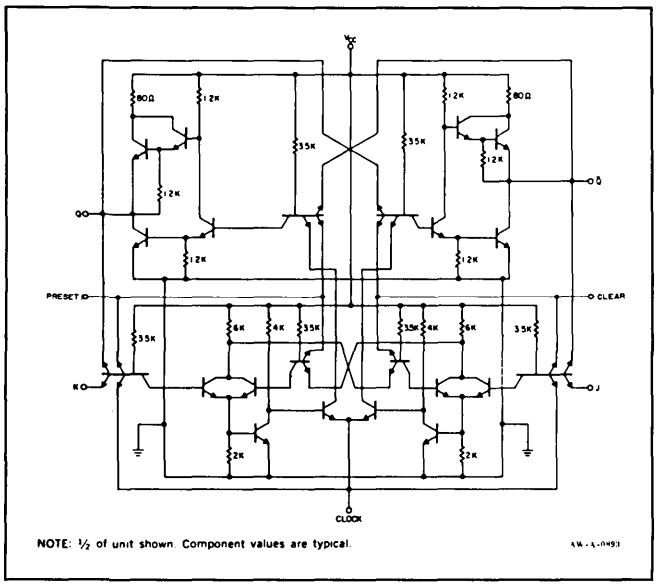
PARAMETER		TEST CONDITIONS ‡		MIN.	TYP.	MAX.	UNIT
$V_{out(0)}$	Logical 0 output voltage	V_{cc} = Min.	I_{sink} = 16mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at D	V_{cc} = Max.	V_{in} = 0.4V			-3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{cc} = Max.	V_{in} = 0.4V			-6.4	mA
$I_{in(1)}$	Logical 1 level input current at D	V_{cc} = Max.	V_{in} = 2.4V			80	μA
$I_{in(1)}$	Logical 1 level input current at clock	V_{cc} = Max.	V_{in} = 2.4V			160	μA
I_{OS}	Short-circuit output current †	V_{cc} = Max.	V_{out}=0 T_A = 25°C	-18		-75	mA
I_{cc}	Supply current	V_{cc} = 5V	T_A = 25°C		35		mA

† Not more than one output should be shorted at a time.
‡ For conditions shown as MIN or MAX, use values specified in "V_{cc} MIN/MAX" table above.

S5476B
N7476B

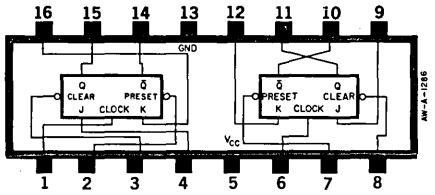
DUAL J-K MASTER-SLAVE FLIP-FLOP WITH PRESET AND CLEAR

BASIC CIRCUIT SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

B PACKAGE



POSITIVE LOGIC

Low input to preset set Q to logical 1
Low input to clear sets Q to logical 0
Clear and preset are independent from clock

LOGIC

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Notes:

1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

DESCRIPTION

The S5476B/N7476B J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows (see Figure 1):

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

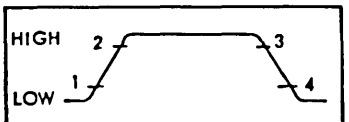


Figure 1 —Flip-Flop Clock Waveform

V_{CC} MIN/MAX

ELEMENT	MIN.	NOM.	MAX.	UNIT
S5476B	4.5	5	5.5	V
N5476B	4.75	5	5.25	V

RECOMMENDED OPERATING CONDITIONS

Width of Clock Pulse, $t_{p(clock)}$ . . . . . $\geqslant$ 20ns
Width of Clear or Preset Pulse . . . . . $\geqslant$ 25ns
Input Setup Time, t_{setup} . . . . . $\geqslant$ Applied Clock Pulse Width
Input Hold Time, t_{hold} . . . . . $\geqslant$ 0

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS ‡		MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{cc} = Min		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{cc} = Min.				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{cc} = Min.	I_{load} = −400μA	2.4	3.4‡		V
$V_{out(0)}$	Logical 0 output voltage	V_{cc} = Min.	I_{sink} = 16mA		0.18‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	V_{cc} = Max.	V_{in} = 0.4V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear, preset, or clock	V_{cc} = Max.	V_{in} = 0.4V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{cc} = Max.	V_{in} = 2.4V			40	μA
$I_{in(1)}$	Logical 1 level input current at clear, preset, or clock	V_{cc} = Max.	V_{in} = 2.4V			80	μA
I_{OS}	Short-circuit output current †	V_{cc} = Max.	V_{in} = 0 T_A = 25°C	−18		−75	mA
I_{cc}	Supply Current (each flip-flop)	V_{cc} = 5V	V_{in} = 5V		8		mA

† Not more than one output should be shorted at a time.
‡ These typical values are at V_{cc} = 5V, and T_A = 25°C.
‡ For conditions shown as MIN or MAX, use value specified in "V_{cc} MIN/MAX" table above.

SWITCHING CHARACTERISTICS, V_{cc} = 5V, T_A = 25° C, and N = 10

PARAMETER		TEST CONDITIONS	TEST FIGURE	MIN.	TYP.	MAX.	UNIT
f_{clock}	Maximum clock frequency	C_1 = 15pF	5	10	15		MHz
t_{pd1}	Propagation delay time to logical 0 level from clear or preset to output	C_1 = 15pF	5		26	50	ns
t_{pd0}	Propagation delay time to logical 1 level from clear or preset to output	C_1 = 15pF	5		34	50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_1 = 15pF	5	10	26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_1 = 15pF	5	10	34	50	ns

S5491
N7491

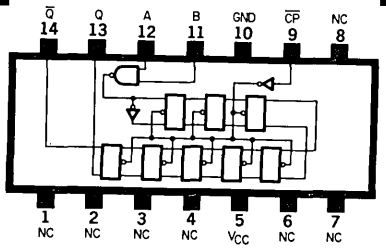
8-BIT SHIFT REGISTER

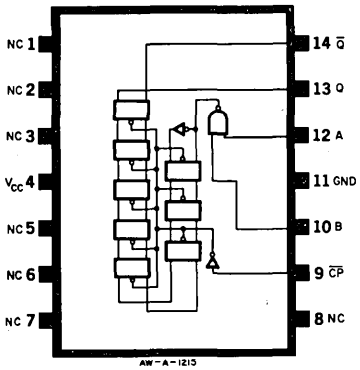
DESCRIPTION

The S5491/N7491 is a monolithic serial-in, serial-out 8-bit shift register utilizing high-speed transistor-transistor logic (TTL) circuits. The shift register, composed of eight R-S master-slave flip-flops, includes input gating and a clock driver. The register is capable of storing and transferring data at clock rates up to 18 MHz while maintaining a typical noise-immunity level of 1 volt. Power dissipation is typically 175 milliwatts, and full fan-out of 10 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B, and $\overline{CP}$) appear as only one TTL input load.

The clock pulse inverter/driver causes the S5491/N7491 to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift-register to be fully compatible with the S5470/N7470 flip-flop and the S5474/N7474 dual D-type flip-flop.





S5491/N7491

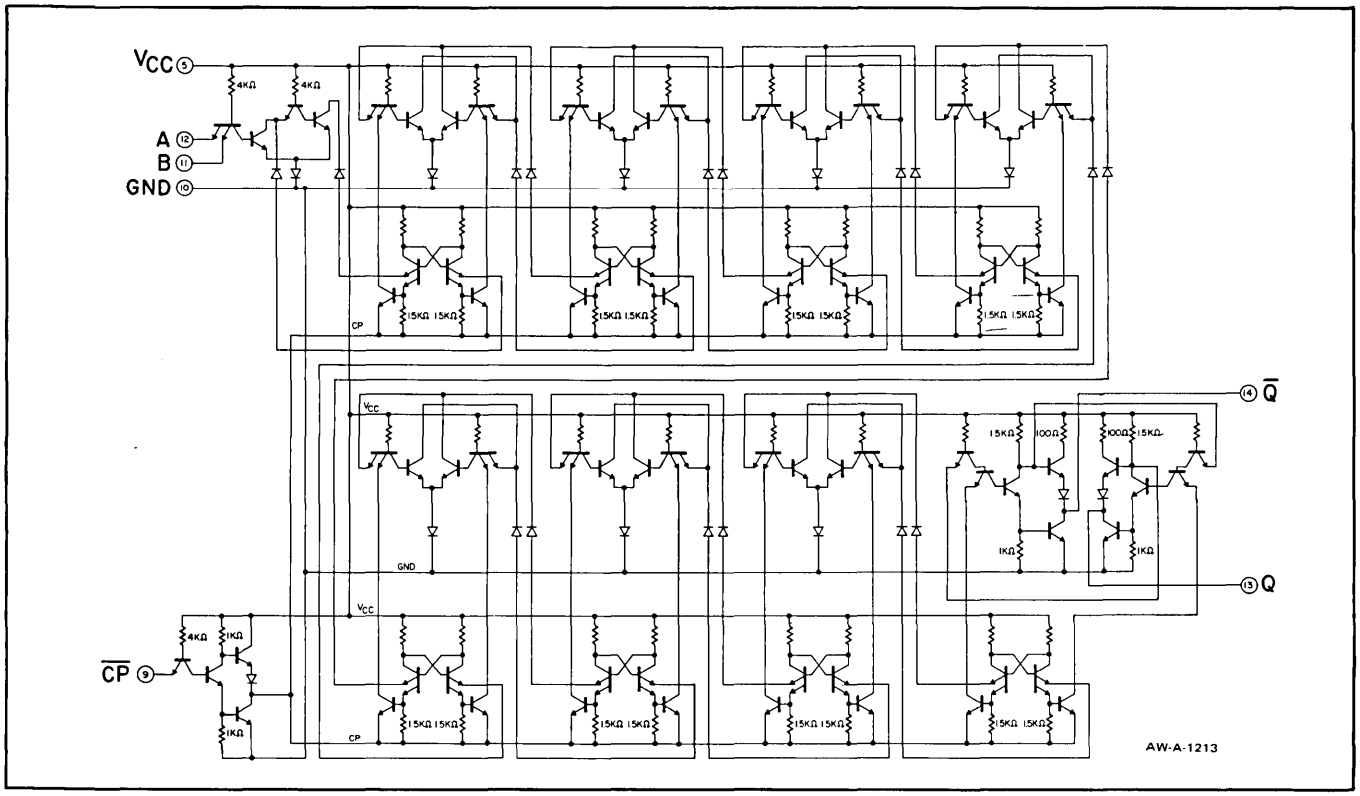
TRUTH TABLE		
t_n		t_{n+8}
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+8} = bit time after 8 clock pulse.

V_{CC} MIN/MAX.

ELEMENT	MIN.	NOM.	MAX.	UNIT
S5491	4.5	5	5.5	V
N7491	4.75	5	5.25	V

8-BIT SHIFT REGISTER



SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C (See Figures 8, 9, and 10)

PARAMETER		MIN.	TYP.	MAX.	UNIT
f_{max}	Maximum shift frequency	10	18		MHz
$t_{p(clock)}$	Minimum clock pulse width		18	25	ns
$t_{setup(0)}$	Minimum logical 0 level setup time required at A or B inputs		12	25	ns
$t_{setup(1)}$	Minimum logical 1 level setup time required at A or B inputs		15	25	ns
$t_{hold(0)}$	Logical 0 level hold time required at A or B input †		−15	0	ns
$t_{hold(1)}$	Logical 1 level hold time required at A and B input		−12	0	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level (clock-to-output)		24	40	ns
$t_{pd(0)}$	Propagation delay time to logical 0 level (clock-to-output)		27	40	ns

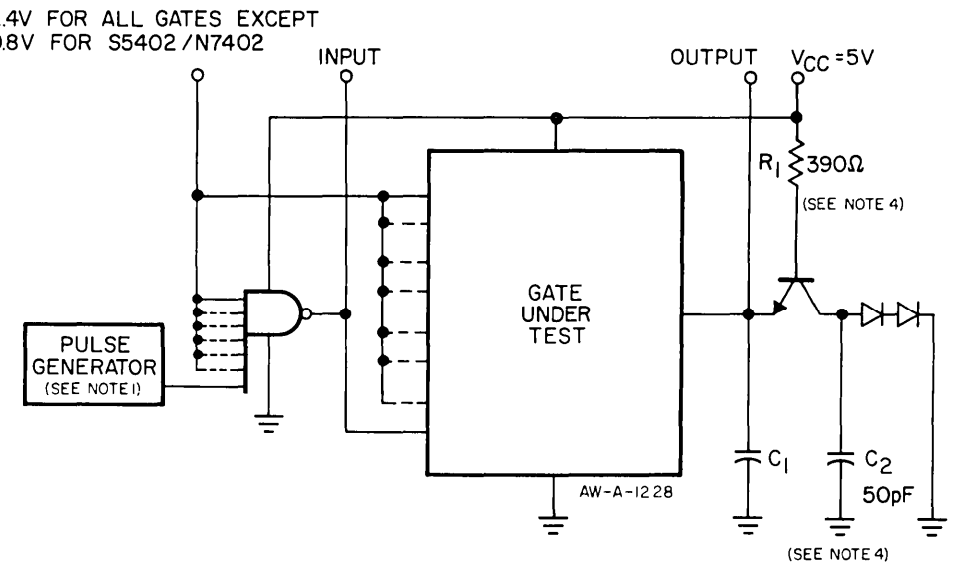
† When the unused input is at logical 1.

ELECTRICAL CHARACTERISTICS

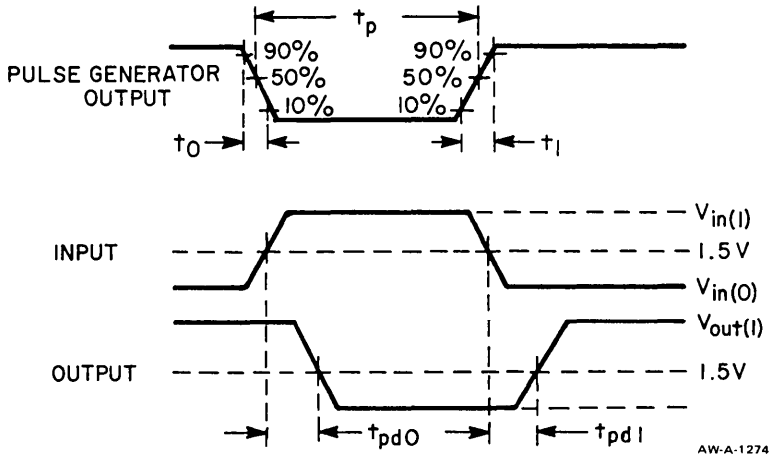
PARAMETER		MIN.	TYP.	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage	2			V
$V_{in(0)}$	Logical 0 input voltage			0.8	V
$V_{out(1)}$	Logical 1 output voltage (N = 10)	2.4			V
$V_{out(0)}$	Logical 0 output voltage (N = 10)			0.4	V
$I_{in(1)}$	Logical 1 level input current at any input			40	μA
$I_{in(0)}$	Logical 0 level input current at any input			−1.6	mA
I_{OS}	Short-circuit output current	−18		−55	mA
I_{CC}	Supply current (T_A = 25°C)		35	70	mA

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS



TEST CIRCUIT



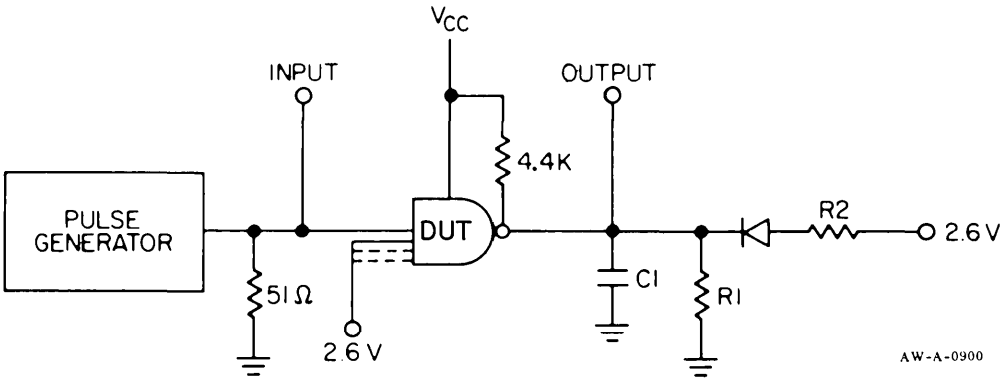
VOLTAGE WAVEFORMS

NOTES:
1. The generator has the following characteristics:
   $t_0 = t_1 \leqslant 15$ns, $t_p = 0.5\mu$s, PRR = 1MHz, $Z_{out} \approx 50\Omega$.
2. All transistors are 2N2368, selected for an inverse β of < 0.1.
3. All diodes are 1N916.
4. Test S5440/N7440 with $R_1 = 130\Omega$, $C_2 = 150$pF.
5. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
6. C_1 includes probe and jig capacitance.

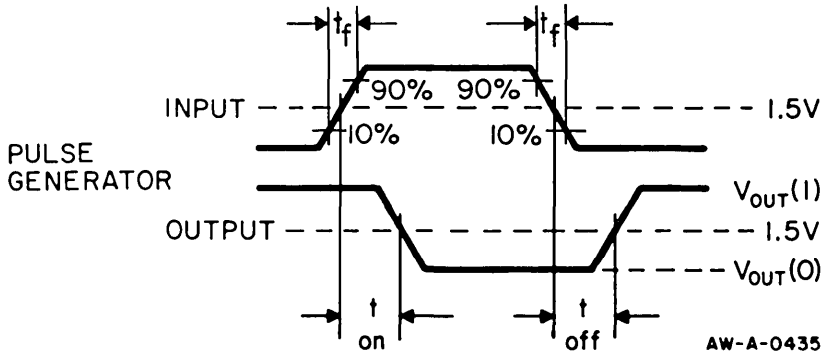
Figure 1-A — Gate Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



TEST CIRCUIT



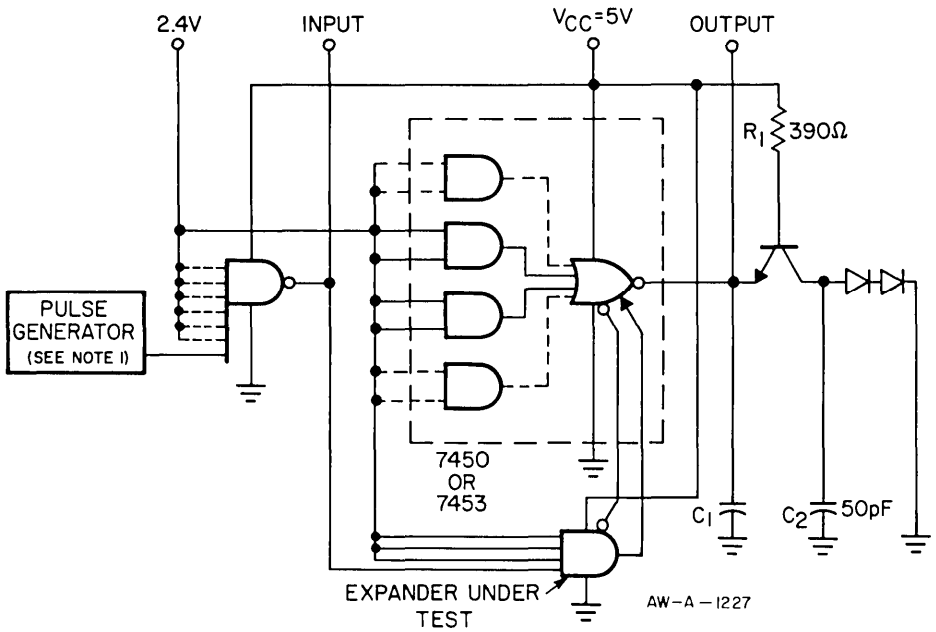
VOLTAGE WAVEFORMS

NOTES: Input Pulse: Amplitude = 2.6V, P.W. = 200ns, $t_r = t_f = 5ns$

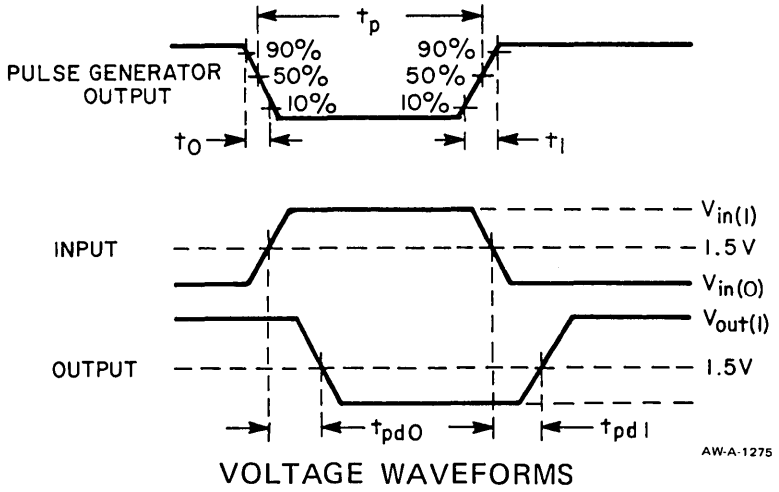
Figure 1-B — Gate Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics:
$t_0 = t_1 \leqslant 15ns$, $t_p = 0.5\mu s$, PRR = 1MHz, $Z_{out} \approx 50\Omega$.

2. All transistors are 2N2368, selected for an inverse β of < 0.1.

3. All diodes are 1N916.

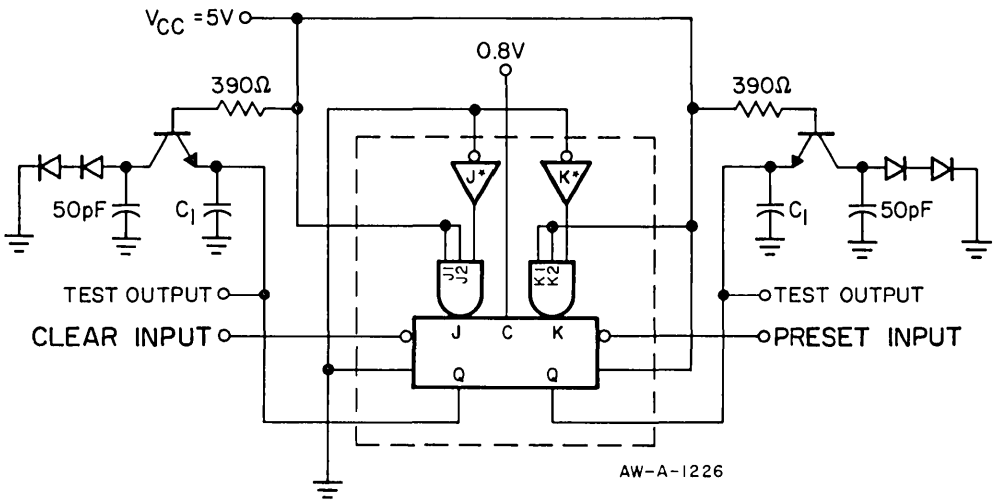
4. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$

5. C_1 includes probe and jig capacitance.

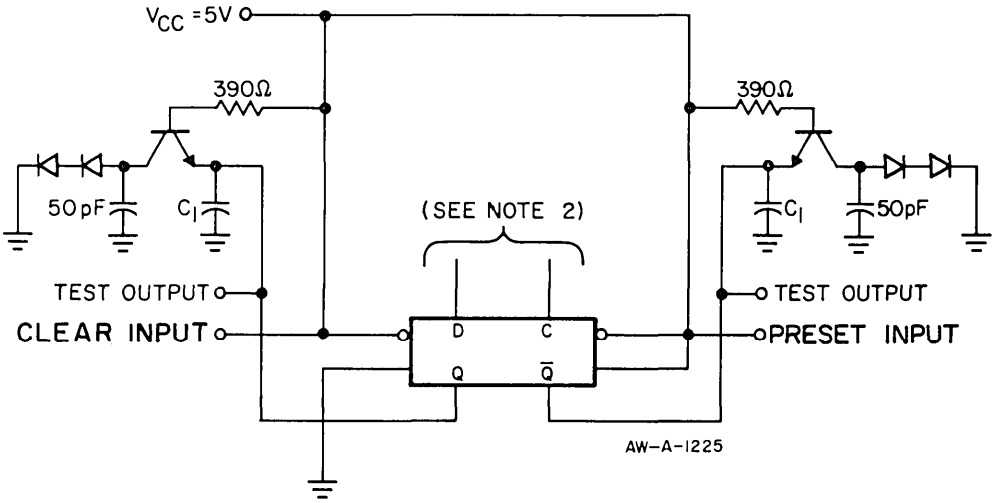
Figure 2 – Expander Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



TEST CIRCUIT
S5470/N7470



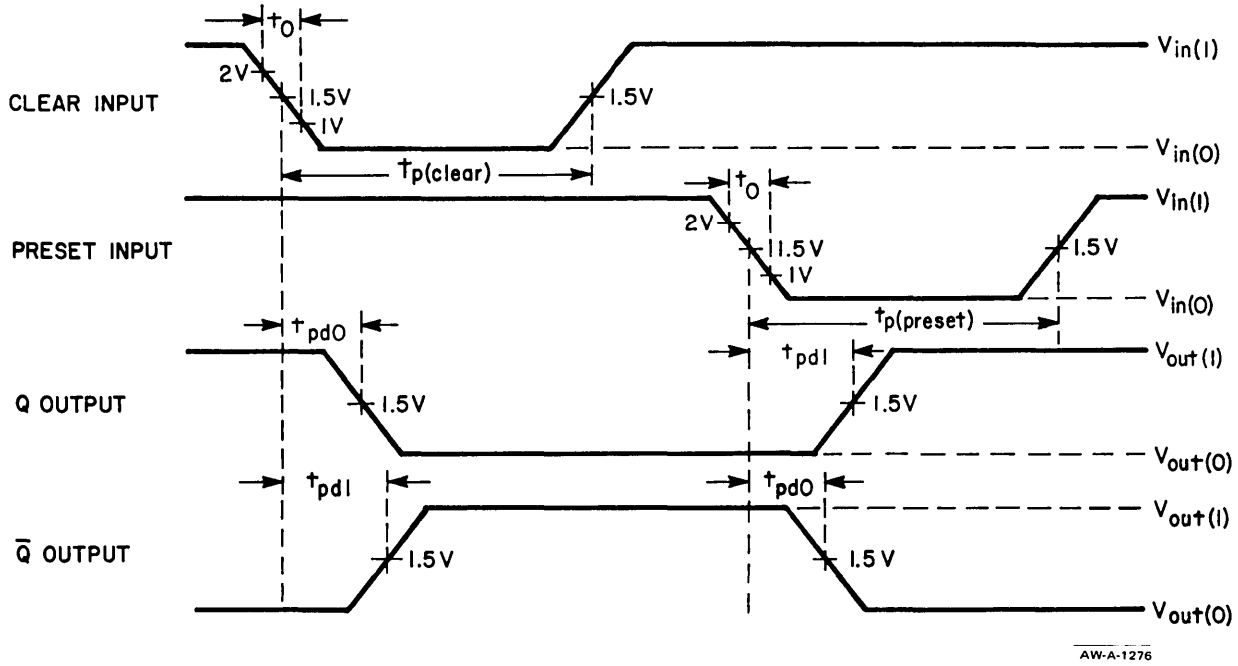
TEST CIRCUIT
S5474/N7474

NOTES:
1. Preset or clear function of the S5470/N7470 can occur only when clock input is low. Gated inputs are inhibited.
2. Clear and preset inputs of the S5474/N7474 dominate regardless regardless of the state of clock or D inputs.
3. All transistors are 2N2368, selected for an inverse β of < 0.1.
4. All diodes are 1N916.
5. C_1 includes probe and jig capacitance.

Figure 3A — S5470/N7470 and S5474/N7474 Preset/Clear Propagation Delay Times.

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



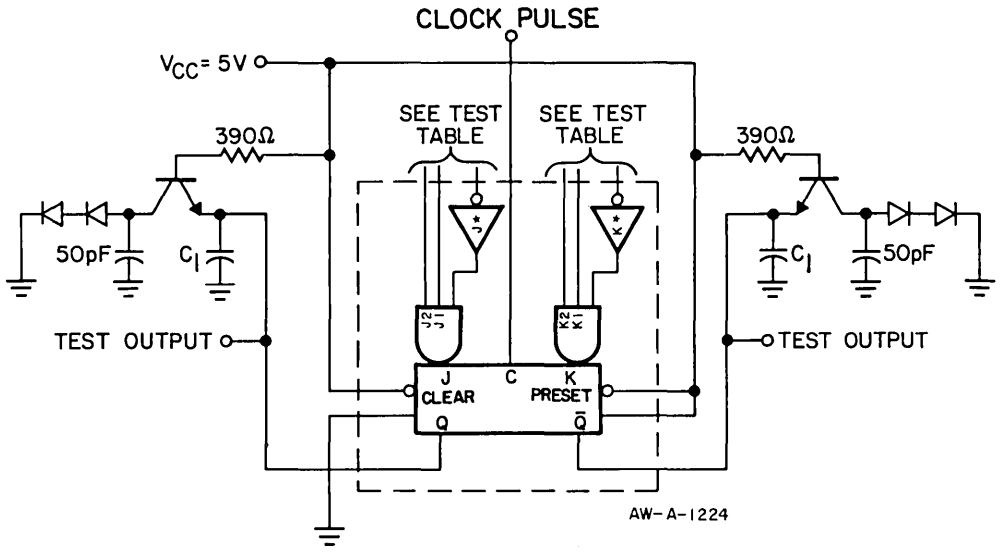
VOLTAGE WAVEFORMS

NOTES: Clear or preset input pulse characteristics:
$V_{in(0)}$ = 0.4V, $V_{in(1)}$ = 2.4V, t_0 = 3 to 6ns,
t_p = 25ns for the S5470/N7474 and
t_p = 30ns for S5474/N7474.

Figure 3B – S5470/N7470 and S5474/N7474 Preset/Clear Propagation Delay Times.

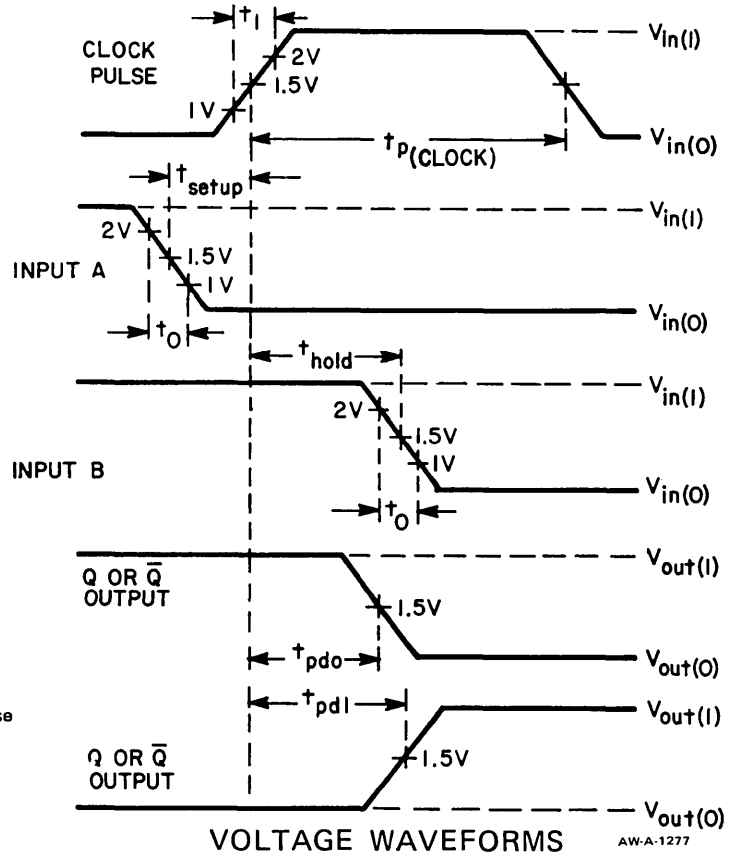
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



TEST CIRCUIT

TEST TABLE					
TEST NO.	TEST	INPUT A	INPUT B	APPLY +2.4V	GND
1	t_{setup} at J*	J*	None	J1, J2, K1, K2	K*
2	t_{hold} at J1, J2	None	J1, J2	K1, K2	J* and K*
3	t_{setup} at K*	K*	None	J1, J2, K1, K2	J*
4	t_{hold} at K1, K2	None	K1, K2	J1, J2	J* and K*

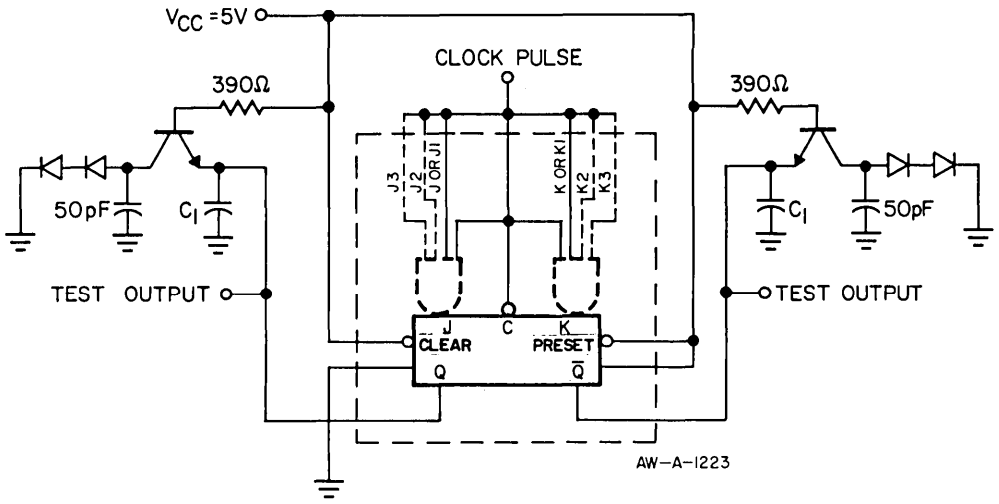


NOTES:
1. Clock pulse (see note 3), input A, and input B are used to measure t_{setup} and t_{hold}.
2. Clock frequency, t_{pd1}, and t_{pd0} (from clock to output) are measured in the toggle mode. Hold J = K = logical 1 per truth table and apply clock pulse (see note 3).
3. Clock pulse characteristics: $V_{in(0)}$ = 0.4V, $V_{in(1)}$ = 2.4V, t_1 = 15ns, t_p = 20ns, and PRR = 1MHz. When testing f_{clock}, vary PRR.
4. Input pulse characteristics: $V_{in(0)}$ = 0.4V, $V_{in(1)}$ = 2.4V, t_0 = 3 to 6ns.
5. All transistors are 2N2368, selected for an inverse β of < 0.1.
6. All diodes are 1N916.
7. C_1 includes probe and jig capacitance.

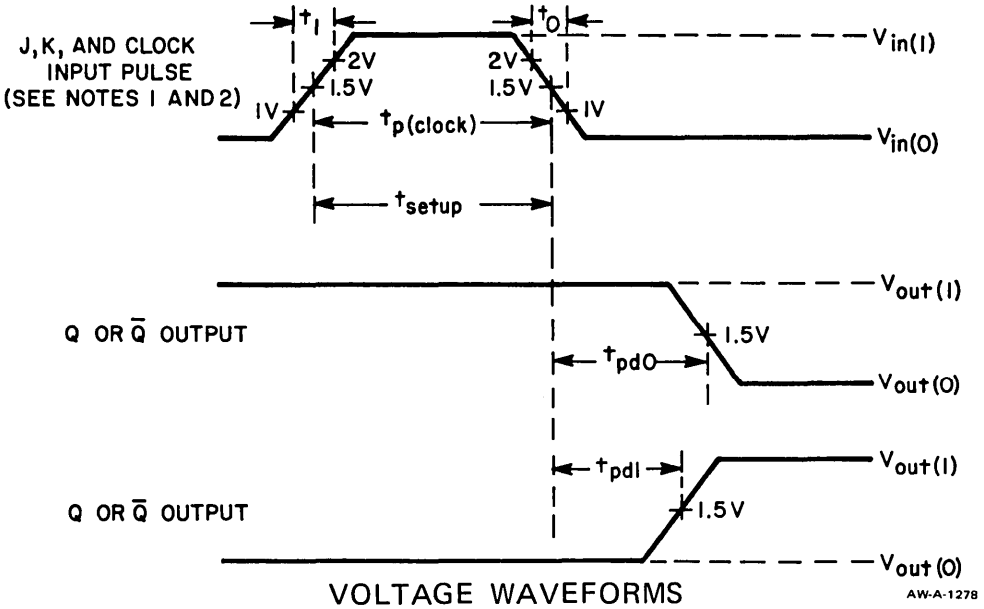
Figure 4 — S5470/N7470 Flip-Flop Switching Times

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



TEST CIRCUIT



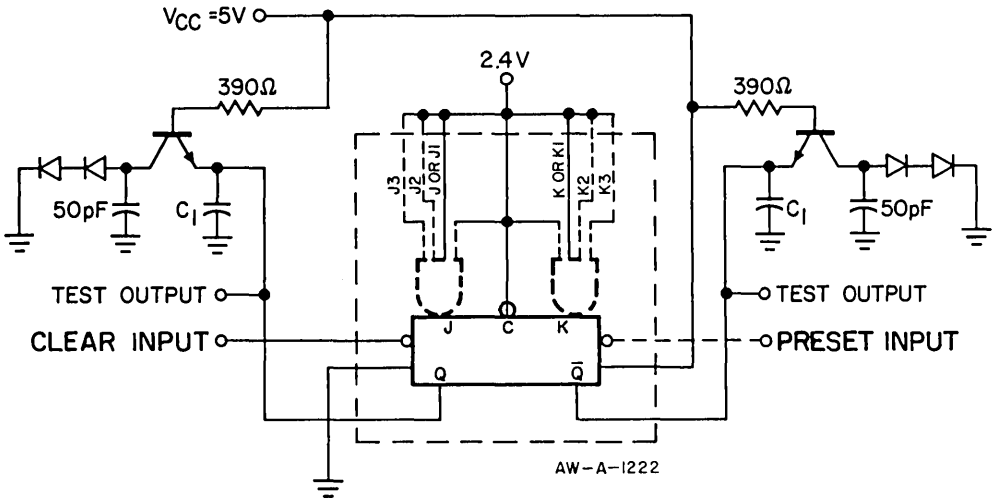
VOLTAGE WAVEFORMS

NOTES:
1. Clock, J, and K input pulse characteristics: $V_{in(0)}$ = 0.4V, $V_{in(1)}$ = 2.4V, $t_1 = t_0$ = 15ns, t_p = 20ns, and PRR = 1MHz. When testing t_{clock}, vary PRR.
2. For the S5472/N7472, J = J1 • J2 • J3 and K = K1 • K2 • K3.
3. Gated inputs (shown with dotted lines) are for the S5472/N7472.only. The S5473/N7473 Dual Flip-Flop has direct J and K inputs and and preset is not available.
4. All transistors are 2N2368, selected for an inverse β of < 0.1.
5. All diodes are 1N916.
6. C_1 includes probe and jig capacitance.

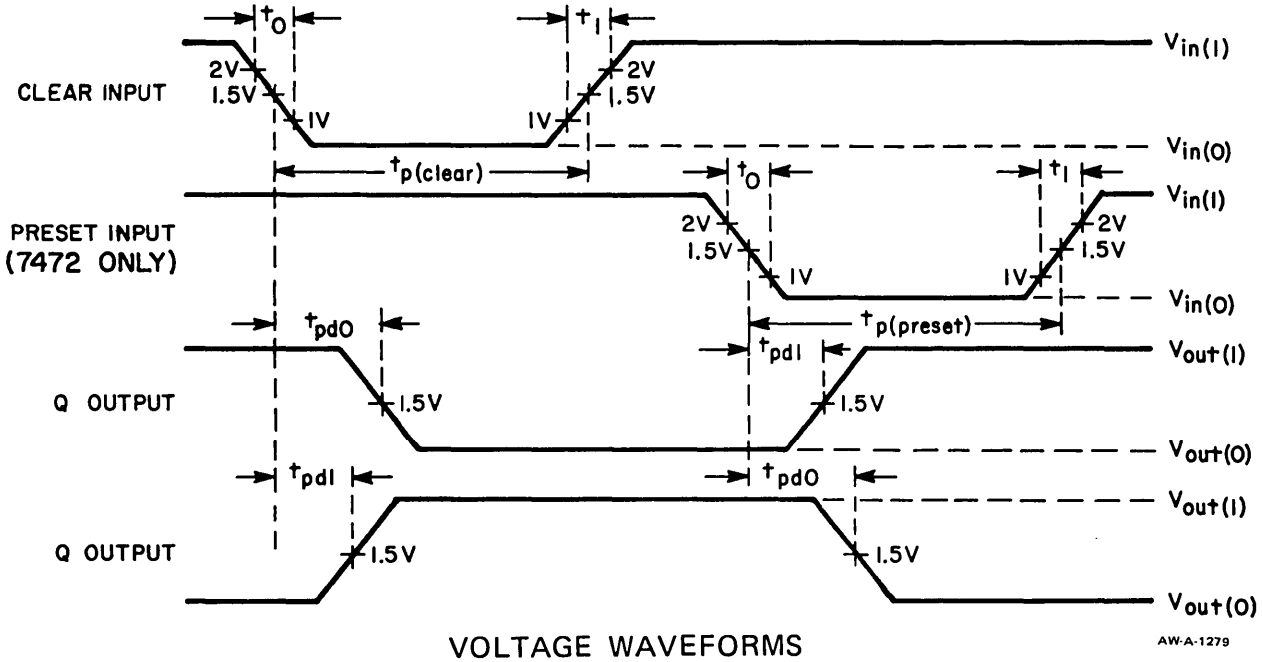
Figure 5 — S5472/N7472, S5473/N7473 , S5476/N7476 Flip-Flop Switching Times

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



TEST CIRCUIT



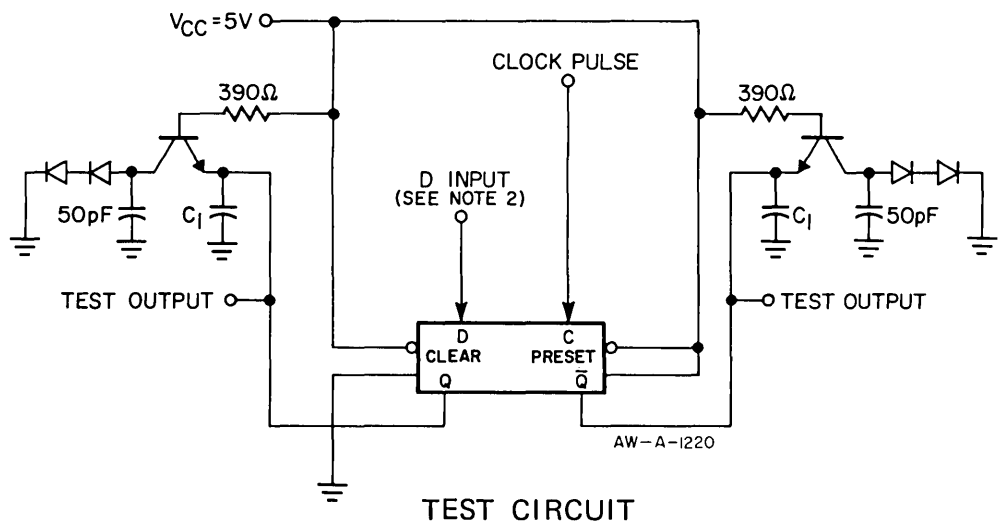
VOLTAGE WAVEFORMS

NOTES:
1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. Clear or preset input pulse characteristics: $V_{in(0)}$ = 0.4V, $V_{in(1)}$ = 2.4V, $t_1 = t_0$ = 15ns, $t_{p(clear)} = t_{p(preset)}$ = 25ns, and PRR = 1MHz.
3. Gated inputs (shown with dotted lines) are for the S5472/N7472 only. The S5473/N7473 Dual Flip-Flop has direct J and K inputs and preset is not available.
4. All transistors are 2N2368, selected for an inverse β of < 0.1.
5. All diodes are 1N916.
6. C_1 includes probe and jig capacitance

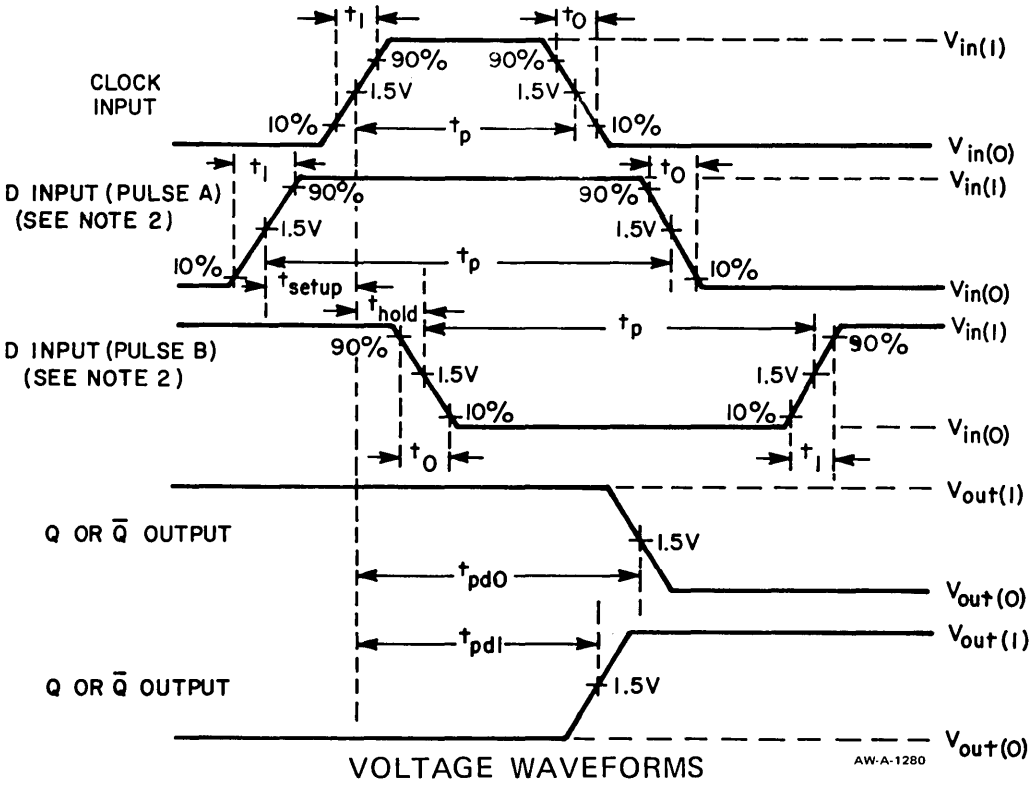
Figure 6 – S5472/N7472 and S5473/N7473 Preset/Clear Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



TEST CIRCUIT



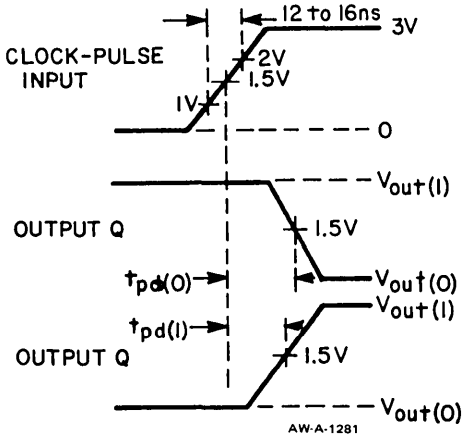
VOLTAGE WAVEFORMS

NOTES:
1. Clock input pulse has the following characteristics: $V_{in(0)}$ = 0.4V, $V_{in(1)}$ = 2.4V, $t_1 = t_0$ = 15ns, t_p = 30ns, and PRR = 1MHz. When testing f_{clock}, vary PRR.
2. D input (pulse A) is used to measure t_{pd1} at Q and t_{pd0} at $\overline{Q}$. Pulse B is used to measure t_{pd1} at $\overline{Q}$ and t_{pd0} at Q. D input (pulse A) has the following characteristics: $t_1 = t_0$ = 15ns, t_{setup} = 20ns, t_p = 60ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: $t_1 = t_0$ = 15ns, t_{hold} = 5ns, t_p = 60ns, and PRR is 50% of the clock PRR.
3. All transistors are 2N2368, selected for an inverse β of $\leq$ 0.1.
4. All diodes are 1N916.
5. C_1 includes probe and jig capacitance.

Figure 7 — S5474/N7474 Flip-Flop Switching Times

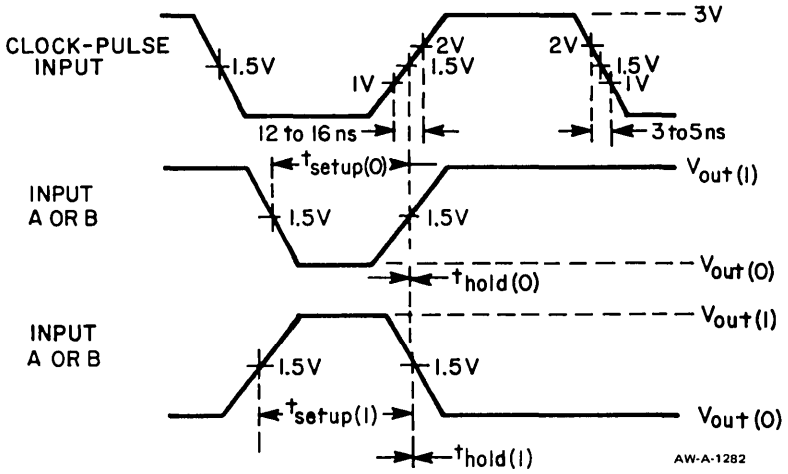
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



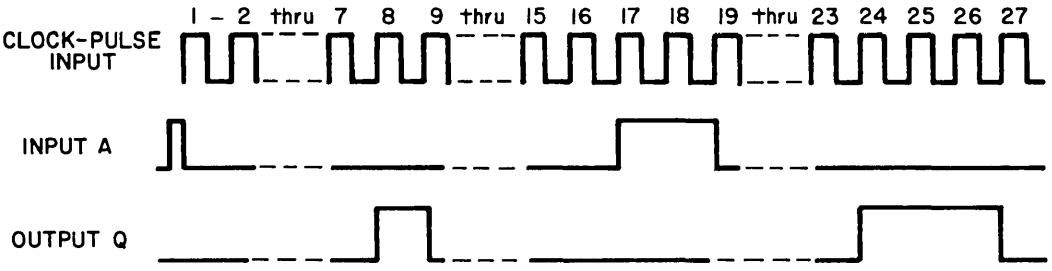
NOTE: The clock-pulse has the following characteristics: PRR = 1MHz and duty cycle = 50%.

Figure 8 - Propagation Delay Times, Voltage Waveforms, for S5491/N7491



NOTES:
1. Each input is tested separately.
2. Unused input is connected to 2.4V.
3. The clock-pulse has the following characteristics: PRR = 1MHz and duty cycle = 50%.

Figure 9 — Switching Times Voltage Waveforms

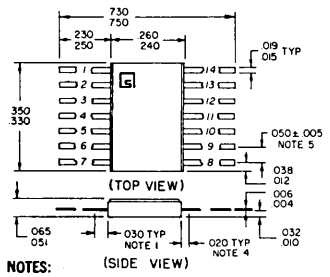


NOTE: Input B is connected to 2.4V.

Figure 10 - Typical Input/Output Waveforms, S5491/N7491

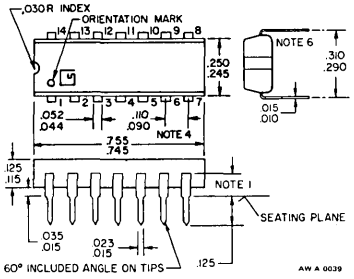
"S" = -55°C to +125°C "A" = 14-pin dual in-line silicone package (TO-116) "N" = 0°C to +75°C "B" = 16-pin dual in-line silicone package "J" = 14-pin flat-pak (TO-88)

J-PACKAGE (TO-88)



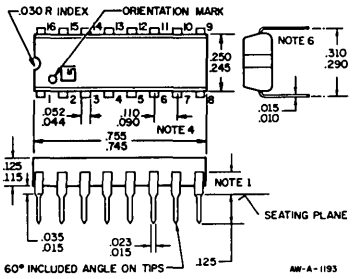
NOTES:
(1) Recommended minimum offset before lead bend.
(2) All leads weldable and solderable.
(3) All dimensions in inches.
(4) Lead spacing dimensions apply to this area only.
(5) Spacing tolerances non-cumulative.
(6) Thermal resistance from junction to still air, $\Theta_{J\text{-}A}$ = 0.3°C/mW.

A-PACKAGE (TO-116)



NOTES: (1) Lead spacing shall be measured within this zone.
(2) Molded Plastic Body.
(3) Kovar Leads.
(4) Lead spacing tolerances are non-cumulative.

B-PACKAGE



(5) Thermal resistance from junction to still air, $\Theta_{J\text{-}A}$ = 0.16°C/mW.
(6) Leads shown as positioned by Signetics dual in-line package carrier.
(7) All dimensions of plastic package exclude molding-caused flash.

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